Design of a PC-Programmable Chip for Hearing-Testing

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by

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Abstract

The design of PC-programmable chip is intended for testing hearing impairedness in a laboratory environment. It is used to feed sound waves of different frequencies and different sound pressure level (SPL) to each ear. The device input is the 12-bit data and 7-bit control signal from USB connection while the output signal is sound waves with frequency range from 20 Hz to 20 KHz. This device is designed and simulated in 0.18 μm CMOS technology.

The chip is intended to fit on a 32 Ω headphones and powered by 1.3V battery. It is designed without ADC and DAC converters. We designed PWM generator using high speed (1 GHz) counter and a digital comparator to achieve more accuracy and reliability than its analog counterpart. A 244 KHz sampling frequency for second order low-pass filter is used to reduce noise and distortion. The output SPL is PC controllable from 1 to 109 dB SPL using USB connection. The control step of 0.5 - 2 dB SPL for 15 to 109 dB SPL range is achieved. This PC controlled device offers flexibility, portability and better controllability of the output sound waves in a hearing impairedness testing laboratory. The improved designs of 12-bit high-speed counter, clock divider and control are also presented.

Keywords: VLSI design, Hearing-Testing, Counter, Clock generator, Clock Divider, Pulse Width Modulator (PWM), Class – D amplifier

To

My Parents,

Nilkanthbhai & Devyaniben

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Nomenclature

ADC	-	Analog-to-Digital Converter
ANSI	-	American National Standards Institute
BJT	-	Bi-polar Junction Transistor
BTE	-	Behind the Ear
CMOS	-	Complementary Metal Oxide Silicon Field-Effect Transistor
D/A	-	Digital-to-Analog Converter
DAC	-	Digital-to-Analog Converter
DFF	-	D Flip-Flop
DLL	-	Delay Locked Loop
DSP	-	Digital Signal Processing
dB	-	Decibel
GHz	-	Giga-Hertz
HA	-	Hearing aid
Hz	-	Hertz
IC	-	Integrated Circuit
IEC	-	International Electro-technical Commission
ITE	-	In the Ear
KHz	-	Kilo-Hertz
MIPS	-	Million Instructions per Second
MOS	-	Metal Oxide Silicon
MOSFET	-	Metal Oxide Silicon Field-Effect Transistor
MUX	-	Multiplexer
NMOS	-	N-channel Metal Oxide Silicon Field-Effect Transistor
PC	-	Personal Computer
PLL	-	Phase Locked Loop
PMOS	-	P-channel Metal Oxide Silicon Field-Effect Transistor
PWL	-	Piece Wise Linear
PWM	-	Pulse-Width Modulator / Pulse-Width Modulated
RMS	-	Root Mean Square
SPL	-	Sound Pressure Level
SoC	-	System On a Chip
TG	-	Transmission Gate
THD	-	Total Harmonic Distortion
TSMC	-	Taiwan Semiconductor Manufacturing Company
USB	-	Universal Synchronous Bus
VLSI	-	Very Large Scale Integrated Circuit
XNOR	-	Exclusive NOR
XOR	-	Exclusive OR

Chapter 1

Introduction

The PC-programmable chip is used for testing hearing-impairedness in a laboratory environment. The chip feeds sound waves with different frequencies and different sound pressure levels (SPL) to each ear. The response of each ear for specific frequency and SPL is recorded on an audiogram. This audiogram is used to program a hearingaid.

The development of a single-chip device for hearing-testing is not designed yet. However, the development of single-chip hearing aids has attracted researchers since long. This resulted in evolution of single chip hearing aid design with different revolutionary techniques. Here, our main objective is to use such revolutionary techniques to implement single-chip device for hearing-testing.

The basics of hearing loss, hearing aid and hearing testing will be helpful in understanding the device for hearing-testing. Then, the comparison of hearing aid and device for hearing-testing is followed by different revolutionary design techniques used for hearing aids.

1.1 Basics of Hearing-Loss, Hearing aid and Hearing-Testing

Hearing loss is defined as the degradation of a person's ability to hear. This hearing loss can be result of many different causes, each having a different effect on one's ability to hear. The most common form of hearing loss is related to the aging process. Impaired hearing usually is the result of a breakdown of the sensory nerve fibers inside the inner ear. Most of the hearing impairment occurs at high frequencies [1].

One might think the primary function of a hearing aid is to compensate for the

loss of sensitivity of the impaired ear. The ear, however, behaves differently for soft sounds near the hearing threshold than it does for loud sounds. This means that a frequency response that restores normal hearing thresholds for soft sounds will not usually be appropriate for louder sounds. Other problems also include the difficulty a hearing impaired listener has for understanding speech in background noise.

At high intensities, loudness is about the same for the hearing impaired and the normal hearing listener. At soft signal levels the loudness becomes more of a function of the hearing threshold. This threshold is much higher for the hearing impaired listener. Simple amplification of all signals will raise the high intensity signals as much as the low intensity signals, causing complaints that the hearing aid is too loud from the user, even though it is working as designed at lower levels [2].

A variety of devices are now available to assist people with a hearing impairment, ranging from simple amplifiers for those with a mild loss, to sophisticated cochlear implant (CI) and auditory brainstem implant systems for those with a profound or total loss. Although these devices provide satisfactory performance for many of their users, few, if any, can restore all the characteristics of hearing to normal. Much of the current research in this field is focused on developing advanced sound processing techniques that are designed to compensate for the perceptual deficiencies that are commonly associated with a loss of hearing sensitivity.

The basic problems encountered in the design of hearing aids may be summarized as follows:

- There are large individual differences in anatomy leading to large deviation in sound pressure at the inner ear.
- The range of acoustic environments is vast. The hearing aid has to process all the sounds which the user is exposed to.
- The hearing aid must have periodic service (battery charging). This is a nuisance to the user and should preferably be done at large time intervals.

Accurately characterizing a hearing aid requires a number of tests. The frequency response is probably its most important characteristic, since it is often directly related to the hearing loss. To determine whether a frequency response varies as a function of input sound pressure level (SPL), measurements are typically made at a number of input SPLs.

Traditionally, frequency response measurements have been made using pure-tone stimulus. ANSI (American National Standards Institute) and IEC (International Electro-technical Commission) standards [3], [4], [5] describe these methods in detail. To measure the hearing impairedness accurately for different frequency and different SPLs, we need accurate and reliable hearing-testing device. The purpose of hearing aid is fruitful only if we measure the hearing-impairedness correctly and accurately.

1.2 Comparison of the Device for Hearing-Testing with Hearing aid

Generally, hearing aids are used to assist hearing of a hearing-impaired person. On the other hand, hearing-testing devices are used to measure the hearing-impairedness at different frequencies and different SPLs in laboratory environment. If we closely observe both the devices, we can see that the main difference in the two is the source of sound signal. Input sound signal in hearing aid is coming from surrounding which is captured by microphone. This audio signal is processed and amplified using class – D amplifier. This processed and amplified audio wave is presented to ear using speaker.

On the other hand, for hearing-testing device, the input sound signal is coming from either audiometer or personal computer (PC). This sound signal is controlled by operator for different frequencies and SPLs. This input sound signal can be either in analog (from spectroscope) or digital (for PC) form. This signal is then processed and amplified using class – D amplifier. And like hearing aids, this signal is then reflected to ear using headphone.

The differences and similarities in both devices are summarized as follows.

1.2.1 Differences in the Device for Hearing-Testing and Hearing aids

Main difference in hearing aid and device for hearing-testing is the method of control. In hearing aid devices, the sound is controlled as per the person's hearing-impairedness. The behavior of person's impairedness is tested before and ear response is obtained using audiogram. The control is designed according to the ear response curve which is unique for each person. On the other hand, in device for hearing-testing, the sound is externally controlled by an operator. The controllable range of frequency can be

from 20 Hz to 20 KHz and controllable range of SPL can be from 0 to 120 dB SPL. This difference exists because the device for hearing-testing is designed for testing hearing-impairedness of any impaired person.

The second difference is the input signal processing. For hearing aids, a microphone is required to convert sound waves to electrical energy. On the other hand, in hearing-testing devices the sound waves are fed from an audiometer or PC.

1.2.2 Similarities in the Device for Hearing-Testing and Hearing aids

The signal processing and amplifier stages are similar in both devices. In the signal processing block, the signal is processed in appropriate form to use as input to the class – D amplifier. The class – D amplifier consists of three stages namely, modulation, amplification and demodulation. The sound waves or digital data for sound are converted into PWM pulses. These PWM pulses are then amplified using an amplifier stage to supply required SPL across speakers or headphones. This amplified PWM pulses are again converted to sinusoidal sound waves. The class – D amplifier is used vastly in both hearing aids and hearing-testing devices because of its very high efficiency.

Moreover, evolution from multi-chip to single-chip device in hearing aids and the design trends from bi-polar junction transistor (BJT) to MOSFET (Metal-Oxide-Silicon Field-Effect Transistor) in microelectronics should be considered to design single-chip device for hearing-testing.

In the following sections, we will discuss the evolution in hearing aids in micro-electronics area and the latest trends in developing hearing-testing devices. The circuit level improvements in designs should also be considered for state of the art chip.

1.3 Evolution of Hearing aids in Microelectronics Field

Conventional analog hearing assisting devices have in the past, been the only way of a hearing impaired individual, to partially restore their ability to hear. The modern hearing assisting devices grew out of the mid-1940s with the invention of the transistor, which has made it possible to develop small, power-efficient amplifier circuits that can be packaged in a form that fits behind or in the ear. Historically, such devices have been

integrated using bipolar circuit techniques like those in [6]. However, during the last decade, such systems are being implemented through CMOS technologies.

Until the past decade and a half, commercial hearing device technology has developed little beyond simple linear amplification. Reliable and small size requirements, combined with unclear scientific evidence for how to properly compensate for sensorineural hearing loss, kept the sophistication of hearing assisting device signal processing to a minimum. Today, the most sophisticated devices available cover a variety of nonlinear processing architectures for hearing loss compensation and some include simple noise reduction processing. They run on l.0V to 1.5V battery.

Previously, a four-chip hearing aid based on CMOS technology is reported which is electrically programmable [7]. It is projected that a general purpose, non-programmable and low cost CMOS hearing assisting device with high reliability offers an attractive developmental challenge. Another paper reports the realization of a two-chip hearing aid using a low voltage 3-micron CMOS process standardized for digital circuits [8].

The increasing market demand on portable system-on-chip (SoC) applications requires new analog circuit techniques for very low-voltage and low-power operation. In this sense, hearing devices are one of the examples with the strongest supply limitations. Currently, such products can be roughly classified as either digitally programmable analog processors [7] – [15] or embedded DSP platforms [16] – [18].

For both kind of designs, the critical design constrains come from the battery technology itself, which imposes a very low-voltage supply operation (down to 1.1 V) combined with low-power figures in order to extend battery life as long as possible (in practice, around one week). In order to overcome the very low-voltage restriction in CMOS technologies, supply multipliers based on charge pumps like those in [19] can be used. In most cases, doublers are included to boost the nominal voltage supplied by the single battery, so that the internal operation of analog parts is at double of the supply voltage. Most of the CMOS designs reported in literature for either digitally programmable analog [7] – [15] or fully digital [16] – [18] hearing assisting devices follow this workaround. Unfortunately, supply multipliers tend to increase both die area and the number of discrete components around the SoC. Also, power efficiency may be

strongly reduced in a final product where battery life is critically important. Finally, some state-of-the-art hearing assisting device implementations as in [18] often make use of special CMOS process optimizations (e.g., deep junction isolation between analog and digital sections, low-noise bipolar devices, and low-threshold MOSFETs), which may increase the final integration cost.

Most conventional analog hearing aids do not have the ability to be customized to the hearing loss of the particular individual. They also suffer from the ability to have the response profile customized for several different applications of the user. It has, however, not been a total success, due to the limitations associated with analog systems.

Some analog CMOS integrated circuits offer an attractive potential for the development of digitally programmable analog hearing assisting device. Though majority of hearing assisting devices are matured on BJT technology, there is a considerable interest in developing CMOS option because of inherent advantages in realization of lower power digital control circuits [20]. The key technological consideration in the design of CMOS technology based designs is the realization of the MOS analog circuits operating within prescribed process corners and low battery voltage range of 1.5 V to 1.0 V.

By integrating advantages of digital control and conventional analog approach, researchers shifted their attention to digitally programmable analog processors. Advantages of the digitally programmable analog processors are lower cost and usually lower power consumption. Major changes to the function of an analog signal processor require electronic circuitry to be designed and constructed, which can be particularly demanding if the device must be small enough to be carried or worn by the user. But, these digitally programmable analog processors have limited controllability and flexibility.

On the other hand, embedded DSP platforms need a sound processor based on a general-purpose DSP chip. The processor must be no larger than pocket-sized, so that users can gain experience with new processing schemes in everyday situations away from the laboratory. The power consumption must be low enough to ensure that neither the size of the battery pack nor the frequency of battery changes will be inconvenient for user. The ease of programming and the computational performance must be adequate for

the implementation of schemes that could feasibly be incorporated into digital instruments.

By using digital signal processing, the different components of the audible spectrum can be broken up into several different sections and the sound levels filtered and reinforced to compensate for the impaired hearing of the user. The filtering and augmentation can be tailored in several different profiles to allow the user to switch to the best suited profile for the particular application. Non-linear amplification of the different signals can also be tailored to the individual user's hearing impairments. Embedded DSP platforms can feature more complex processing algorithms and exhibit a shorter time to market.

Digital signal processing (DSP) is preferred over analog processing for one predominant reason: flexibility. Because the functional specification of a DSP device is determined almost entirely by software, new processing schemes can be developed, evaluated, and modified relatively easily [21].

While the introduction of hearing assisting device with DSP chips allow the application of sophisticated signal processing techniques to these devices, their capabilities are still limited by a processing power of a few MIPS (Million Instruction per Second) due to the inherent constraints of a hearing assisting device platform. The ease of programming general-purpose digital processors comes at the cost of high power consumption, and relatively large physical size and weight [22]. Although DSP chips are beginning to appear in hearing aids packaged in conventional behind-the-ear (BTE) and in-the-ear (ITE) enclosures, so far these devices are custom-designed and lack the flexibility required in research. While they are programmable in the sense that a set of parameters can be adjusted to suit the individual user, the processing algorithm is to a large extent embedded in the circuitry, so that major changes are not possible.

1.4 Objectives

As discussed above, there are some key limitations in digitally programmable analog processors and embedded DSP platforms. Therefore, the combination of both devices to achieve the best results for hearing-testing devices should be considered. The

device for hearing-testing should offer very high reliability and flexibility. Other main concerns for the device for hearing-testing are:

- Single chip design
- Single 1.3 V supply without any voltage multipliers
- 20 Hz to 20,000 Hz frequency response
- Accurate control steps with large range of SPL
- Fully Digital PWM generator
- 12-Bit accurate resolution
- Avoid use of any data converts (Analog-to-Digital or Digital-to-analog) and complex DSP algorithms

The CMOS circuit technique should avoid the necessity of any supply multiplier, resulting in a programmable hearing testing device on-chip with internal operation at the true voltage of single-battery supply. Furthermore, the SoC should be fully integrated in a standard CMOS technology without any process enhancement. All elements, with the exception of coupling and bypass capacitors should be contained within the single mixed-signal IC chip. With satisfying all the mentioned needs, the most important concern for device for hearing-testing is reliability, flexibility and controllability. It is intended to fit on 32 Ω head-phone with 1.3 V battery supply. Therefore, the chip-area and low power are also design constraints.

1.5 Designing Tools Used

All individual blocks of the proposed hearing-testing device are implemented in Cadence Design Environment using CMOS 0.18 μm technology for TSMC fabrication process. All the blocks and/or gates are implemented at the transistor level. The hierarchical block for all transistor level implementation is created and used for further higher order blocks. Virtuoso Composer – Schematic Editor is used as schematic editor. The transistor level implementations of all the gates, used in implementation throughout this thesis, are shown in Appendix A. The widths of all NMOS and PMOS transistors are minimum possible for static CMOS implementation. SpectreS simulation tool available in Cadence Design Environment is used to obtain all the simulation results and

waveforms.

1.6 Organization of the Thesis

Chapter 2 highlights the development of the device for hearing-testing and existing designs of main blocks of the device for hearing testing. Two main sections of the device for hearing-testing, namely digital pulse-width modulator and class – D output stage, control and filter, are also discussed with their recent trends. Recent trends of individual blocks are also described. Chapter 2 also describes the block diagram of the proposed PC programmable device for hearing-testing.

In Chapter 3, the digital pulse-width modulator section is discussed in detail. Importance of the blocks in this section (clock generator, clock drive, reset circuits, 12-bit high-speed counter, 12-bit digital comparator and PWM logic) is explained using architecture diagram. The implementation in CMOS 0.18 μm technology is also explained. The authenticity of all the blocks is supported by appropriate simulation results and waveforms.

In Chapter 4, the class – D output stage, control and filter section is discussed. First, the detailed explanation of control for device for hearing-testing is given. The calculations for control design are also derived. The importance of the blocks in this section (control logic, class – D output stage & coarse control, active low-pass filter and fine control) is mentioned by architecture diagram. The implementation is also explained and appropriate simulation results and waveforms are also provided to prove the desired functionality.

In Chapter 5, the complete hearing-testing system is described. All the blocks described in Chapter 3 are combined together to implement the first half (digital pulse-width modulator) of the complete device for hearing-testing. All the blocks described in Chapter 4 are combined together to implement the second half (class – D output stage, control and filter) of the single-chip device. The simulation results for each section are provided.

The thesis is concluded in Chapter 6 by summarizing the contributions made and also by outlining areas for further research.

Chapter 2

Previous Designs of the device for Hearing-Testing and Its Blocks

2.1 Introduction

In this chapter, development of the device for hearing-testing is described. Previous designs of main blocks like Pulse-Width Modulator, class – D output stage and active low-pass filter are discussed. Recent Designs of internal blocks of the pulse-width modulator like clock-generator and counter are described. The recent trends of the designs of class – D output stage and active low-pass filter are also discussed. Finally, over-view of the proposed single-chip design is given.

2.2 Previous Design of the Device for Hearing-Testing

A design of computerized hearing testing system using supervisory control and data acquisition system is described in [23]. This system is designed using the off-shelf components. Therefore, the over all design consists of many IC (integrated circuits) chips. There is no published article for single-chip hearing-testing system.

In the following sections, recent trends in pulse-width modulator, class – D amplifier output stage and active low-pass filter are discussed.

2.3 Previous Designs of Pulse-Width Modulator (PWM)

Pulse-width modulator is one of the important blocks for hearing assisting

devices. In general, the PWM output can be generated by a direct or an indirect approach. The direct approach usually involves two steps as depicted in Figure 2.1.

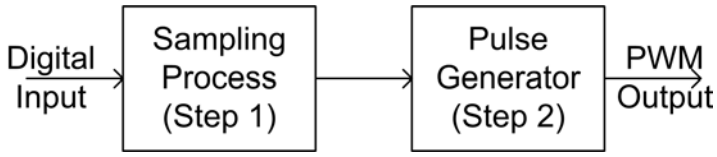


Figure 2.1: PWM Generator using Direct Approach

The first step is a sampling process to determine the digital value of the PWM pulse width that corresponds to the sampled value of the input signal. The second step is to generate the corresponding PWM pulses based on the digital value provided by the sampling process. The indirect approach [24], [25] usually involves a modulation process including over-sampling by interpolation and delta-sigma modulation. The required computation for the indirect method is rather intensive and does not render well for portable power sensitive applications.

There are several methods used to implement pulse-width modulator block [24] - [30]. PWM pulses can be generated using either analog [24] - [28] or digital design techniques [29], [30]. Digital design technique is more preferable than analog design technique because of its higher reliability and accuracy. Pulse-width modulator using data converter (ADC or DAC) [18] and other complex digital design techniques [30] were developed previously. Some PWM generator designs used upto 10-bit counter [29], [30]. The speed of the counter is an important factor to be considered in designing digital PWM generator. In the counter based designs, clock generator is also an important part.

In the following sub-sections, recent trends to design clock generator and counter are discussed in detail.

2.3.1 Clock Generator – Previous Designs and Recent Trends

Some designs of the clock generator are proposed in [31] - [37] based on DLL, PLL, timer and simple digital ring-oscillator. All these designs, except the simple digital ring-oscillator based one, consume more power and area. They are also designed using complex analog or digital design techniques. To avoid complexity and to reduce power

and area, digital ring-oscillator based clock generator design [31] is widely preferred.

Another element to generate the required clock frequency is clock divider. Clock divider designs using digital techniques are mentioned in [38] - [40]. These designs use DFF (D-Flip Flop) and some additional gates to implement the clock divider circuit.

2.3.2 Counter – Previous Designs and Recent Trends

A counter is another important block for generating PWM pulses digitally. The number of bits in counter is limited by the speed to achieve accurate PWM pulses. Therefore, as the speed of the counter increases, the number of bits should also be increased to achieve higher resolution. The speed of the counter depends on critical path delay. Generally, n-bit counters are implemented using n-bit adders and an n-bit register. And hence, fast adder is required for high-speed counter design. The carry-look ahead, carry select and conditional sum based adders are very popular for their high speed. Designs of some adders are described in [41] and [42]. Among them, the conditional sum based adder [42] is very attractive for high speed counter since it has the lowest critical path delay.

2.4 Class – D Amplifier Output Stage – Previous Designs and Recent Trends

In general, the Class D output stage drives a load consisting of a low-pass filter and an output transducer. The methodology to optimize the design of the output stage of the Class D amplifier for maximum power efficiency (with a small IC area) is described in [43]. Digital Class D amplifiers are increasingly prevalent as power amplifiers in audio applications, in particular audio portable devices where the critical parameters include low voltage (1.0V - 1.5V), low power operation and small Integrated Circuit (IC) area. In the digital hearing instrument, total quiescent current budget is very low, and most of the power should be allocated to complex signal processing (such as noise reduction [44]) as opposed to signal conditioning. The Class D amplifier is particularly advantageous in this application [43] since it features high power efficiency (of the order of 90%) over a large modulation index range (signal swing). It also does not need a

digital-to-analog (D/A) converter when interfaced to a digital processor; resulting in power savings and reduced hardware.

2.5 Active Low-pass filter – Previous Designs and Recent Trends

Low-pass filters are familiar devices with wide-spread and varied applications. In different forms, they are used in taking measurements, for restricting noise, for carrier suppression after demodulation, and as a crossover network, to mention just a few applications. The inductor-capacitor (LC) based passive filters have several drawbacks. Although capacitors can be easily fabricated on-chip with higher accuracy, it is more difficult to integrate inductors on-chip because of the required large area. Furthermore, inductors are prone to noise pickup. At low frequencies, it is difficult to procure inductors with sufficiently high Q (Quality factor) to make a filter reliable. Finally, the active filter is smaller and easy to fabricate on-chip. The use of op-amp in active low-pass filter permits fast and simple construction of reliable filter. Active low-pass filters can be implemented on-chip by different available techniques [45]. In 1965, a table to calculate capacitor and resistor values for active low-pass filter was derived [45]. After that, the researchers rapidly developed formulas and algorithms to calculate values of capacitors and resistors for different characteristics of active low-pass filter. Butterworth, Chebyshev and Elliptic filter are very popular active filters. The filter equations for these filters are derived in [46]. Moreover, the low-pass filter equations for different order filter are also derived in [46]. The values of capacitor and resistor for the required specification of an active low-pass filter can also be calculated using the algorithm developed in [46].

2.6 Overview of Proposed Device for Hearing-Testing

The block diagram of the proposed single-chip device for hearing-testing is shown in Figure 2.2.

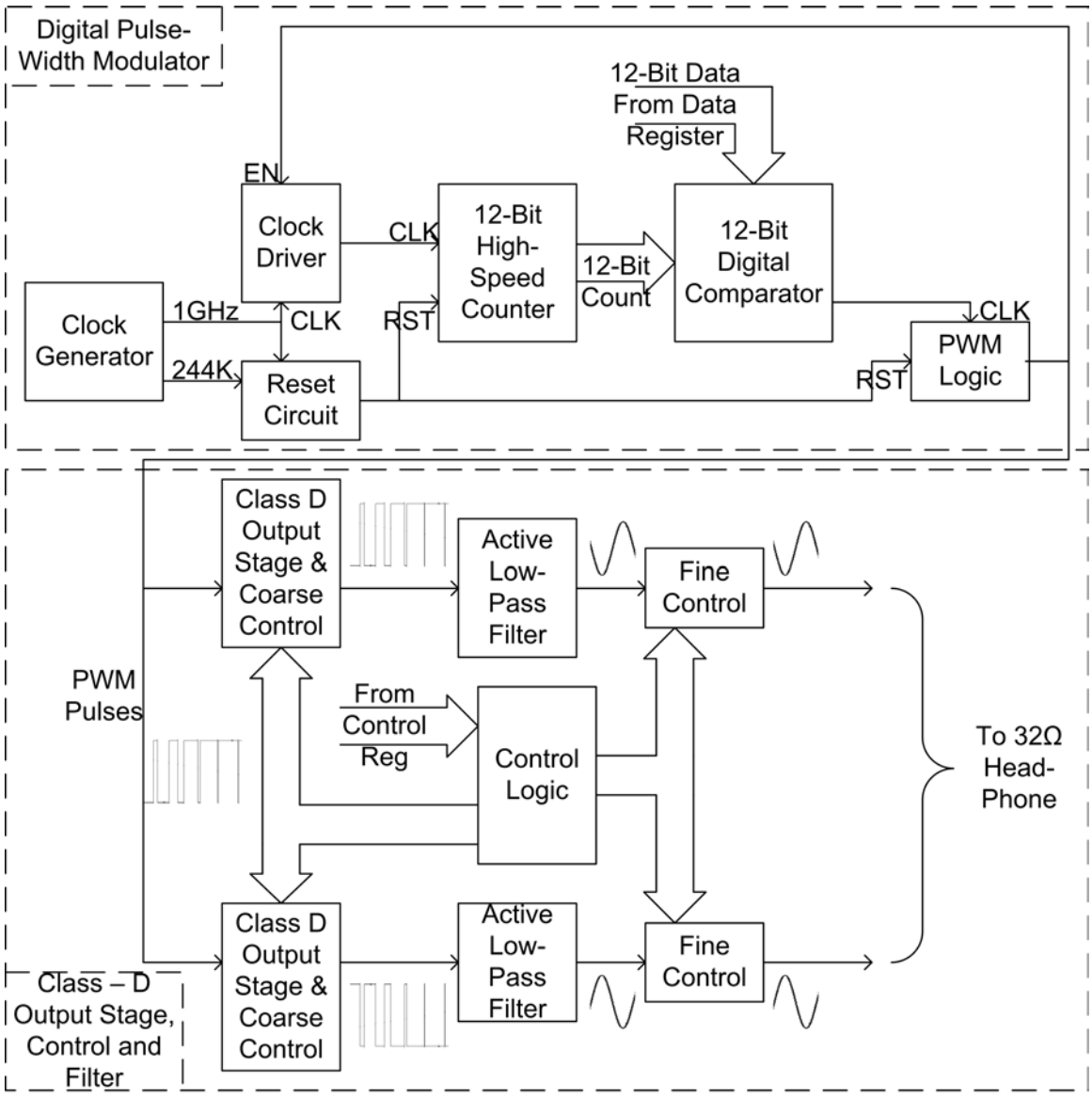


Figure 2.2: Block Diagram of the Proposed Device for Hearing-Testing

Our device for hearing-testing is divided in two main sections separated by dashed rectangles. They are:

- Digital pulse-width modulator, and
- Class – D output stage, control and filter

Main blocks for the digital pulse-width modulator section are:

- Clock Generator
- Clock Driver
- Reset Circuit

- 12-Bit High-Speed Counter
- 12-Bit Digital Comparator, and
- PWM Logic

And main blocks for the class – D output stage, control and filter section are:

- Control Logic
- Class – D Output Stage and Coarse Control
- Active Low-Pass Filter, and
- Fine Control

The designs of all the blocks of the digital pulse-width modulator are described in Chapter 3 and detailed designs of all the blocks of the class – D output stage, control and filter are presented in Chapter 4.

2.7 Summary

First, the previous design of the device for hearing-testing is described. The recent trends to design the pulse-width modulator with appropriate references are also described. The clock generator and counter blocks of the pulse-width modulator are also discussed with previous design techniques. Furthermore, the previous designs of the class – D output stage and active low-pass filter are also described. Finally, the block diagram of the proposed design of the chip for hearing-testing with sections and blocks is given.

Chapter 3

Design of Digital Pulse-Width Modulator

3.1 Introduction

In this chapter, the detailed design of the digital pulse-width modulator section of the device for hearing-testing will be described. First, overview of the digital pulse-width modulator will be given. Then, all the blocks of the digital pulse-width modulator section will be described in detail. Block level architecture, transistor level implementation and simulation results for each block will be explained.

3.2 Overview of Digital Pulse-Width Modulator

The digital pulse-width modulator is first of the two sections of the single-chip device for hearing-testing. This section is designed to generate PWM pulses from 12-bit digital data provided from PC. The 12-bit digital data represents sound signals from 20 Hz to 20 KHz. The main blocks of the digital pulse-width modulator section are clock generator, clock driver, reset circuit, 12-Bit high-speed counter, 12-bit digital comparator and PWM logic. The block diagram of the digital pulse-width modulator is shown in Figure 3.1.

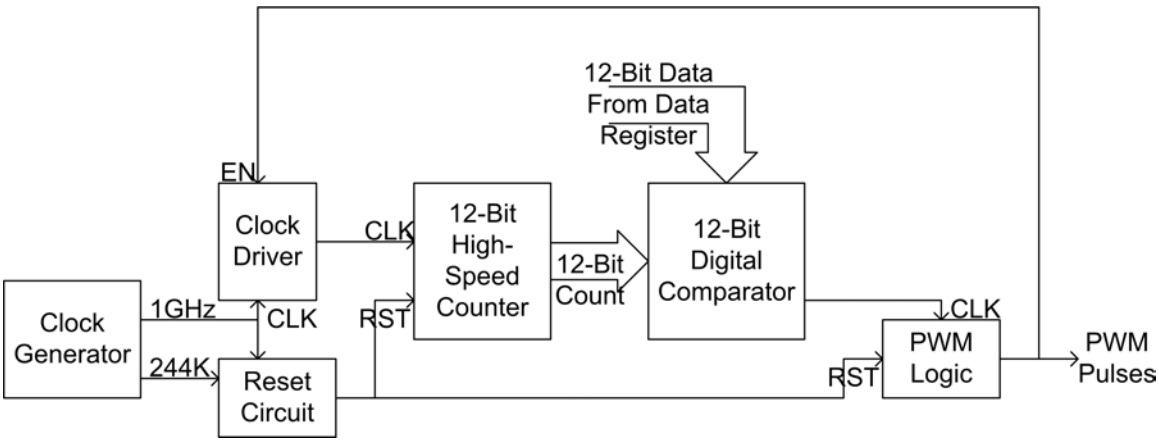


Figure 3.1: Block Diagram of the Digital Pulse-Width Modulator

The general operation of the digital pulse-width modulator is explained below.

First, the clock generator starts generating 1 GHz and 244 KHz clock signals. On the rising edge of 244 KHz clock, the data in 12-bit data register and 7-bit control register is updated. At the same time, momentary reset pulse resets 12-bit high-speed counter to zero and pulls high the PWM pulse output. The 12-bit high-speed counter starts up-counting. The 12-bit digital comparator compares data register value with up-counter value on every count. The comparator generates momentary low pulse when both digital inputs are equal. The momentary low pulse is latched by PWM logic and hence stops counting in the counter. The cycle continues on every rising edge of 244 KHz clock. In this section, only 12-bit data register is used. 7-bit control register is used in the second section (class – D amplifier output stage, control and filter) of the device for hearing-testing. Main design concerns for the blocks of the digital pulse-width modulator are described briefly in the following paragraphs.

The device for hearing-testing was intended to use 250 KHz sampling frequency and hence clock frequency for 12-bit counter would be 1.024 GHz ($250KHz \times 2^{12}$). The 1.024 GHz frequency is rounded to 1 GHz which resulted in 244 KHz ($1GHz \div 2^{12}$) sampling frequency. Hence, two clock frequencies (1 GHz and 244 KHz) are required which is generated using the clock generator.

The clock driver is designed to save dynamic power by disabling the clock pulses to the counter during low level of PWM pulses. The reset circuit is designed to provide momentary high pulse of 2 ns duration on every rising edge of 244 KHz clock. The

PWM logic block is designed to latch momentary low pulse from 12-bit digital comparator and momentary high pulse from the reset circuit.

All the blocks shown in Figure 3.1 are designed using digital design techniques. Each block of the digital pulse-width modulator will be discussed in the following sections.

3.3 Clock generator

Clock is an important component in any digital circuit. The clock should be accurate for proper functioning of other circuitry. We designed the clock generator using ring-oscillator [31] and clock divider circuits. First, architecture of the clock generator is explained followed by implementation in 0.18 µm CMOS technology. Finally, waveforms and observations obtained from simulations are presented for authenticity of the clock generator design.

3.3.1 Architecture

The architecture and the applications of the clock generator are shown in Figure 3.2:

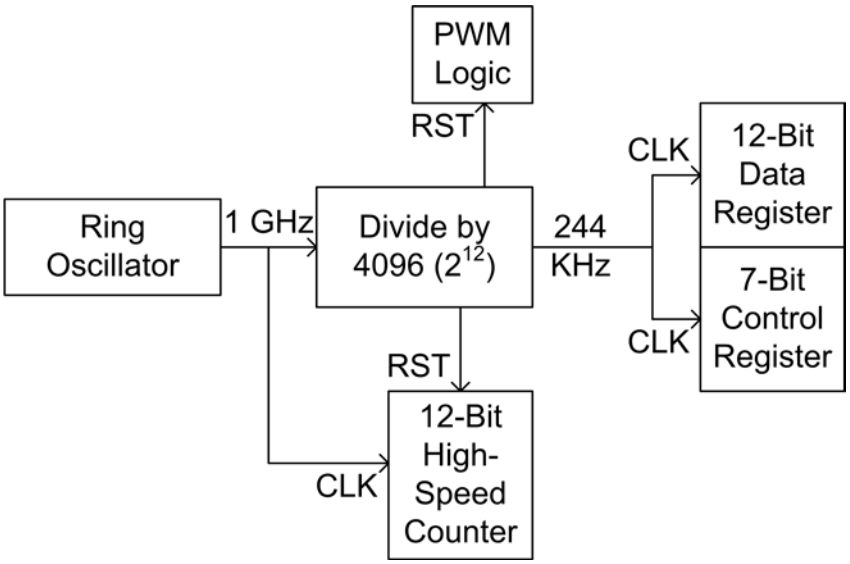


Figure 3.2: Architecture of the Clock Generator

The clock is used for different purposes in different digital design blocks. Two clock frequencies, 1 GHz and 244 KHz, are generated in the clock generator. The 1 GHz clock is used as clock pulse in 12-Bit high speed counter. The 244 KHz clock is used as clock in 12-Bit data register and 7-Bit control register. The 244 KHz clock is also used to reset 12-Bit high speed counter and in the PWM logic.

First, 1 GHz clock is generated using ring-oscillator and 244 KHz clock is generated using 1 GHz clock as reference. In the clock divider, 1 GHz clock is divided by 4096 (2^{12}) to obtain 244 KHz frequency.

3.3.2 Implementation

The clock generator is implemented using two blocks: the ring-oscillator and the clock divider. The top level hierarchical blocks of the clock generator are shown in Figure 3.3.

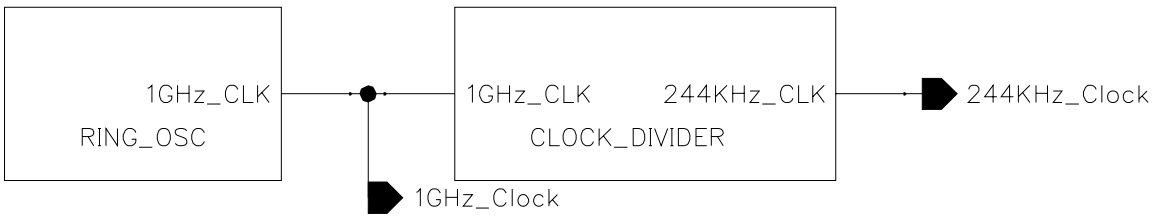


Figure 3.3: Implementation of Top Level Hierarchical Blocks of the Clock Generator

First block of the clock generator is the ring-oscillator. Transistor level implementation of the ring-oscillator is shown in Figure 3.4. The ring-oscillator is an odd number inverter chain which consists of 7-inverters with ascending transistor-widths. The transistor-widths of NMOS and PMOS for the first four inverter stages are 0.22 µm and 0.5 µm respectively. Then, consecutive stages are in ascending order to allow fast charge and discharge of the high capacitance of the 12-Bit high-speed counter, the clock driver and the reset circuit. The transistor-widths of NMOS and PMOS for final stage inverter are 7.5 µm and 15 µm respectively.

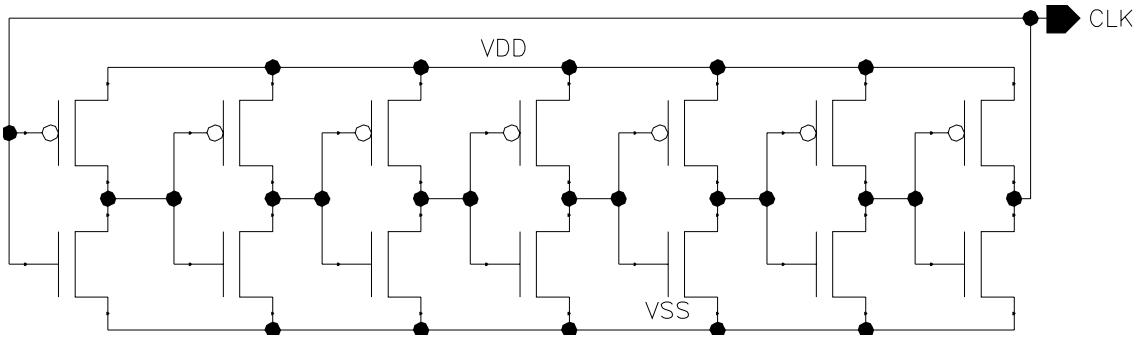


Figure 3.4: Transistor Level Implementation of the Ring-Oscillator

The second block of the clock generator is the clock divider. As shown in Figure 3.5, the clock divider is implemented using rising-edge triggered D flip-flop (DFF). One DFF is required to divide the clock frequency by 2. Therefore, 12-DFF chain is used to divide clock frequency by 4096.

For the first D-FF, the CLK input of D-FF is connected to 1 GHz clock frequency. The Q output is used as output which provides 500 MHz (divide-by-2) clock frequency. The Q' output of DFF is connected back to the D input of the same DFF. Hence, on every rising edge of the CLK input (1 GHz clock), output is inverted at half the frequency (500 MHz) of CLK input (1 GHz). And hence, 500 MHz (divide-by-2) clock is obtained at the Q output.

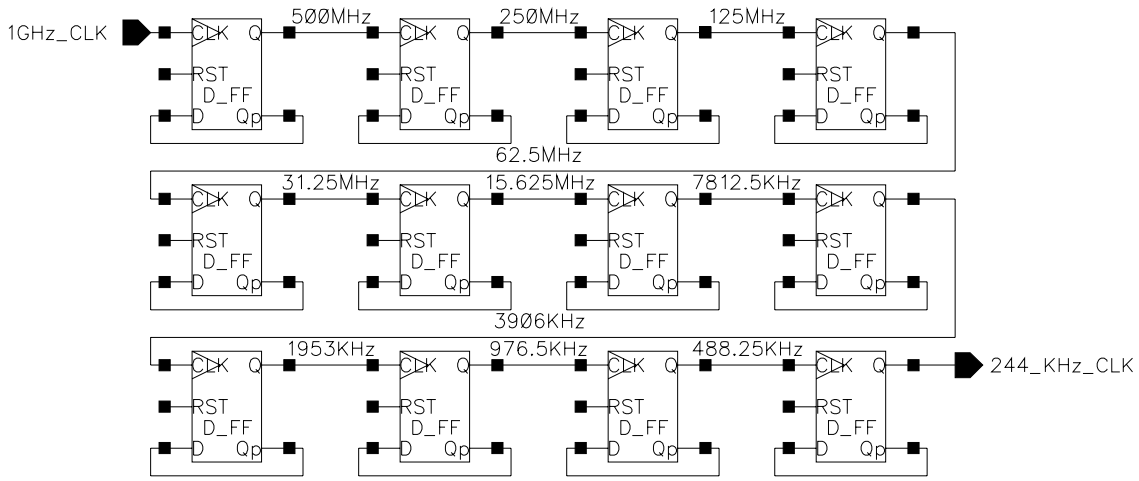


Figure 3.5: Implementation of the Clock Divider

3.3.3 Simulation Results

In this section, we have provided simulation waveforms and results for the 1 GHz and 244 KHz clock frequencies.

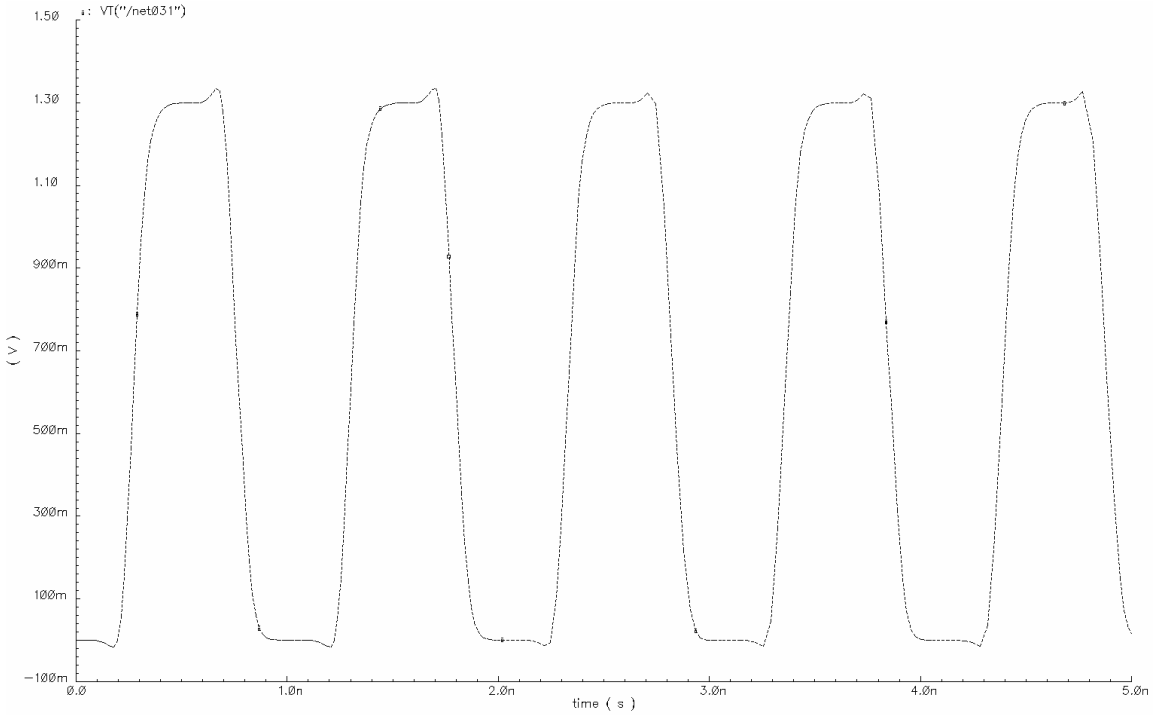


Figure 3.6: Simulation Waveform for 1 GHz Clock

The simulation waveform for the 1 GHz clock is shown in Figure 3.6. The rise and fall time are satisfactory. The voltage swing also represents full swing from 0 V to 1.3 V.

The simulation results for time period, frequency, rise time, fall time and % error for 1 GHz clock is shown in Table 3.1

Details	Observation
Time Period (in nsec.)	1.013
Frequency (in GHz)	0.99
Rise Time (in psec.)	111.96
Fall Time (in psec.)	113.80
% Error in 1 GHz Frequency	**1%**

Table 3.1: Simulation Results for 1 GHz Clock

As shown in Table 3.1, the percentage error in 1 GHz clock frequency is only 1 % which is very good for desired functionality.

The simulation waveform for the 244 KHz clock is shown in Figure 3.7.

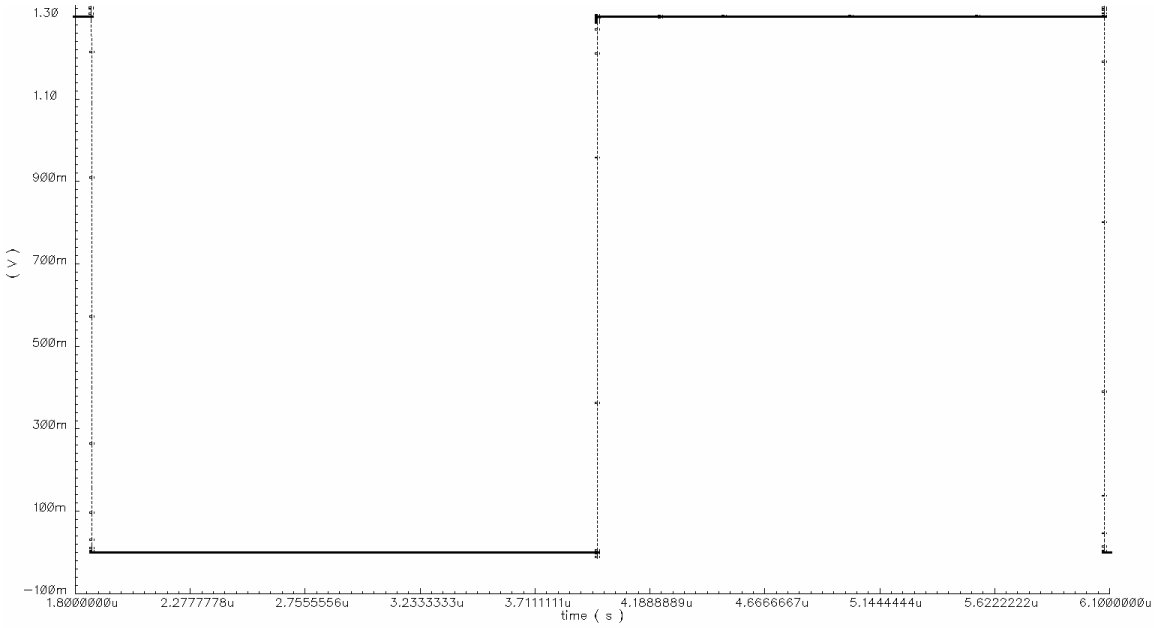


Figure 3.7: Simulation Waveform of 244 KHz Clock

The simulation results for time period, frequency, rise time, fall time and relative error in frequency for the 244 KHz clock is shown in Table 3.2.

Details	Observation
Time Period (in μsec.)	4.1499
Frequency (in KHz)	241
Rise Time (in psec.)	168.68
Fall Time (in psec.)	201.52
% Error in 244 KHz Frequency	**1%**

Table 3.2: Simulation Results for 244 KHz Clock

Therefore, the correct functionality and accuracy of the clock generator block is proved.

3.4 Clock Driver

The clock driver is designed to save dynamic power by stopping the clock driving the 12-bit high-speed counter when PWM pulse is at logic low level. The dynamic power consumption decreases as switching activity decreases. In the proposed design, the 12-bit counter is operating at 1 GHz which is the highest switching activity in the hearing-testing device. Hence, the counter consumes the highest dynamic power. Furthermore, the counter has no significance during low level of the PWM pulses. Hence, by stopping the clock to the counter, we can save dynamic power. The clock is restarted when the PWM pulse goes logic high again.

The clock driver is also used as a buffer between the clock generator and the 12-bit high-speed counter. It is designed such that it can supply the required current to the 12-bit counter.

3.4.1 Architecture

The architecture of the clock driver is shown in Figure 3.8.

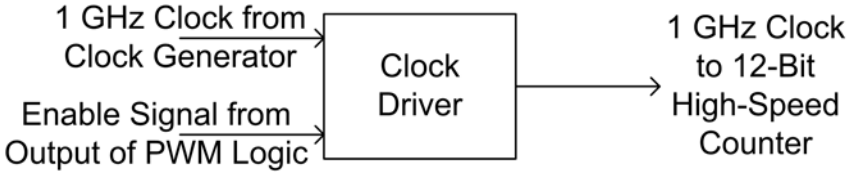


Figure 3.8: Architecture of the Clock Driver

As shown in Figure 3.8, the clock driver is an interface between the clock generator and the 12-bit high-speed counter. It consists of only one logical block. The inputs to the block are 1 GHz clock from the clock generator and enable input from the PWM logic (PWM pulses). The output supplied from the block is the clock signal driving the 12-bit counter. The logic function of the block is explained in the following paragraph.

If the enable input (PWM pulse) to the clock driver is low, the output clock is pulled high regardless of the input clock. Hence, the clock to the counter is disabled. When the enable input goes high, the input clock is inverted and fed at the output which

restarts the counter. Hence, the clock driver works as an inverter when enable signal is logic high.

3.4.2 Implementation

The implementation of the clock driver is shown in Figure 3.9.

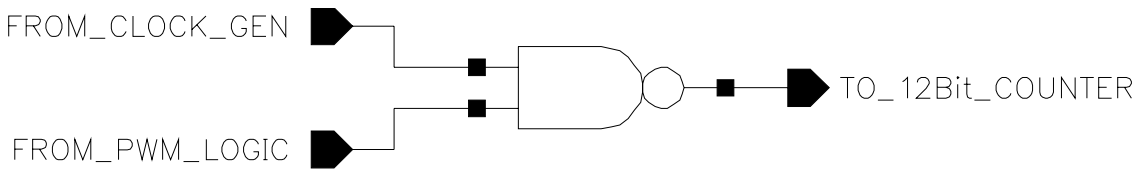


Figure 3.9: Implementation of the Clock Driver

A two input NAND gate is used to implement the clock driver logic as shown in Figure 3.9. The widths of the NMOS and PMOS transistors are 5 μm and 10 μm respectively. The operation of the clock driver is explained below.

When the enable input (from the PWM Logic block) is at logic high level, the output of the NAND gate and hence the clock to the counter depends on the clock input. The clock input is inverted before it is fed to the output. Now, when the enable input is at logic low level, the output of NAND gate is pulled high. When the reset pulse goes logic high for 2 ns, the PWM pulse and hence the enable signal to the clock driver goes high. This recovers the application of the clock signal to the counter.

3.4.3 Simulation Results

The simulation waveform for the clock driver output is shown in Figure 3.10.

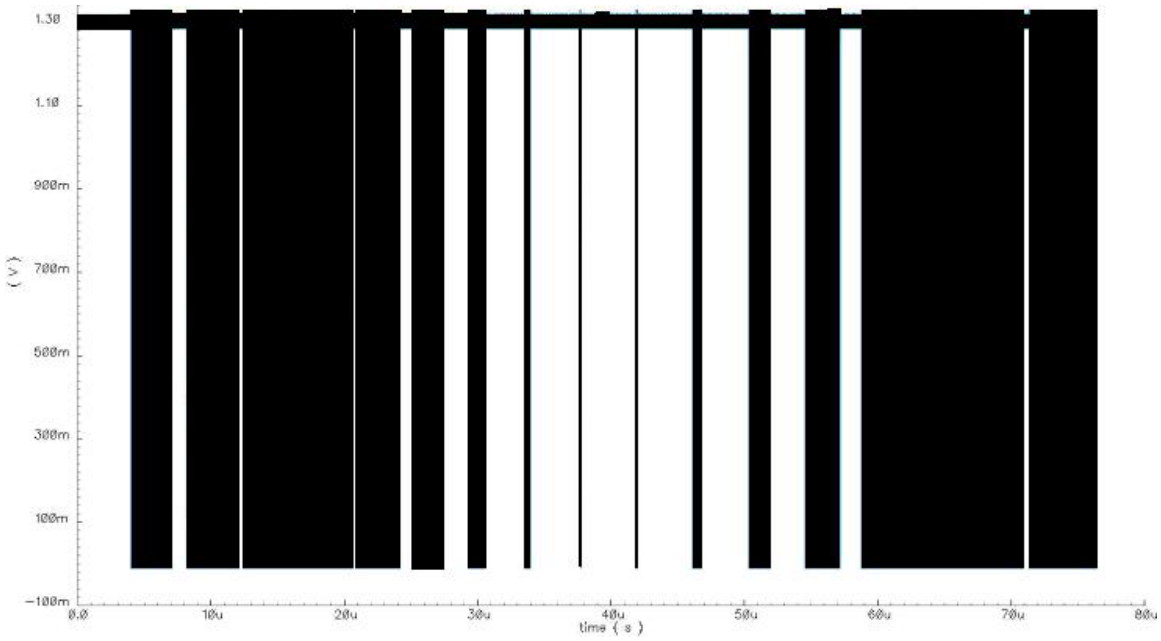


Figure 3.10: Simulation Waveform at Output of the Clock Driver

The ON and OFF states of the clock to the 12-bit counter are clearly visible in Figure 3.10. The duration of ON and OFF time is varying according to the duty cycle of the PWM pulse. The simulation waveform is measured for 76 μs which is more than one cycle for a 20 KHz sound wave.

The dark portion in Figure 3.10 indicates the presence of the clocking activity. The white or blank portion indicates the absence of the clocking activity and the clock is pulled high during this time period.

From the simulation waveform, we can conclude that the switching activity reduction varies with the PWM pulse duty cycle. The authenticity of the logic for the clock driver is verified from the simulation waveform shown in Figure 3.10.

3.5 Reset Circuit

The reset circuit is designed to generate a momentary high pulse on every rising edge of the 244 KHz clock. The duration of the momentary high pulse is 2 ns for robust reset operation. The critical path for the reset operation consists of the reset circuit, the PWM logic and the clock driver logic blocks. For guaranteed clock recovery on every

reset, the duration of the reset pulse should be more than the critical path delay. Hence, the pulse-width of 2 ns for the reset pulse is chosen.

3.5.1 Architecture

The architecture of the reset circuit and its inputs and outputs are shown in Figure 3.11.

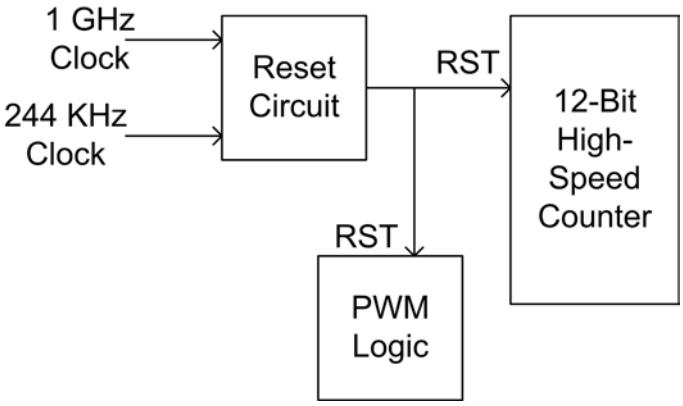


Figure 3.11: Architecture of the Reset Circuit

The 1 GHz and 244 KHz clock signals are used as the input to the reset-circuit block. The 1 GHz clock is used to achieve the accurate delay of 2 ns. The momentary high pulse with 2 ns pulse-width is generated at the output. The reset pulse is used to reset the 12-bit counter to 0 and to pull the PWM pulse high in the PWM logic block.

3.5.2 Implementation

The implementation of the reset circuit using basic digital design blocks is shown in Figure 3.12.

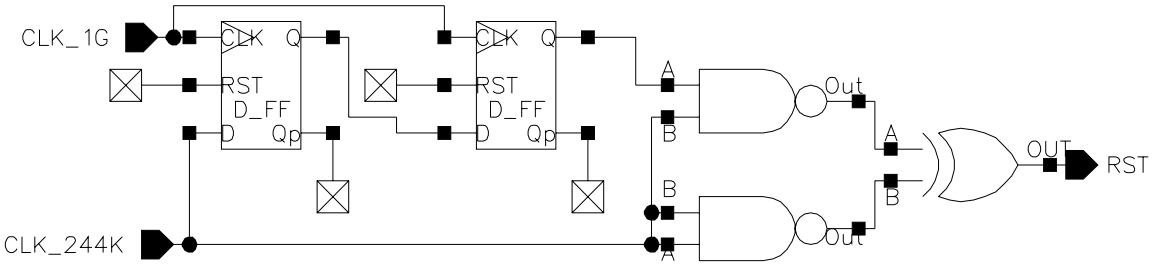


Figure 3.12: Implementation of the Reset Circuit

The reset circuit is implemented using 2 D-Flip-Flops, 2 NAND gates and 1 XOR gate, as shown in Figure 3.12. The 1 GHz clock is used as the clock input to both D-Flip-flops. Hence, each D-Flip-Flop works as a delay element of 1 ns. The widths of all the NMOS and PMOS used in the design are 0.22 µm and 0.5 µm respectively. The operation of the reset circuit is explained below.

At steady logic levels, either '1' or '0', the output of the second DFF and the 244 KHz clock have the same logic level. Hence, both the inputs to the XOR are similar which results in logic low output. When the falling edge at 244 KHz clock is detected, both inputs to the XOR are kept at same logic level by the NAND gates. This results in a logic low output. When the 244 KHz clock is rising, both the NAND gates behave as an inverter. Hence, the inputs to the XOR are '0' and '1' for 2 ns which results in the logic high output for 2 ns. After 2 ns, both inputs to the XOR are logic high again and hence the output goes low.

3.5.3 Simulation Results

The simulation waveforms of input and output of the reset circuit are shown in Figure 3.13.

Figure 3.13(a) shows 244 KHz clock and Figure 3.13(b) shows the output generated from the reset circuit which is the momentary high-pulse with 2 ns pulse-width.

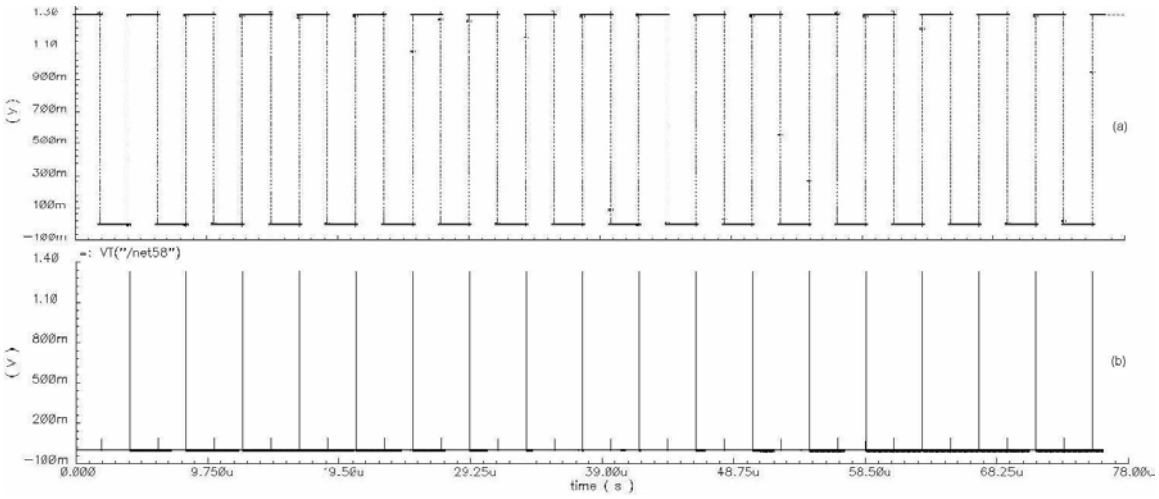


Figure 3.13: Simulation Waveforms (a) 244 KHz Clock and (b) Output of the Reset Circuit

The momentary high-pulses occur on every rising edge of 244 KHz clock without any malfunction. At the steady logic levels and the falling edge, the output remains at logic low level without glitches. The voltage swing at output is also correct. Hence, the simulation waveforms authenticate the operation and validity of the reset circuit.

3.6 12-Bit High-Speed Counter

This is an important block of the digital pulse-width modulator. The block should be designed carefully to achieve the desired functionality. It is a challenge to design efficient 12-bit counter, counting at 1 GHz clock frequency using 1.3 V supply, with low area and low power consumption.

Generally, the counters are designed with high-speed adders and a register. To design fast counter with lower area, the critical path delay of the adder should be minimum. The design of the conditional sum based adder for least critical path delay is published in [42]. The critical path delay for the conditional sum based adder is,

$$(\log_2 W + 1) \bullet t_{mux} \tag{3.1}$$

Where, W is number of bits, and

t_{mux} is propagation delay of 2-to-1 multiplexer

Therefore, for 12-bit /16-bit, the critical path delay remains the same, which is equal to

$$5 \bullet t_{mux} \tag{3.2}$$

The number of multiplexers required for the adder in [42] is,

$$(W \log_2 W + 1) \tag{3.3}$$

Where, W is number of bits in the adder

Therefore, for 12-bit design, total 49 2-to-1 multiplexers are required.

For the counter, the input is incremented by '1' on every clock cycle. This functionality is achieved by connecting one of the two inputs of the adder to logic low and the carry input to logic high.

3.6.1 Architecture

The architecture of the 12-Bit high-speed counter is shown in Figure 3.14.

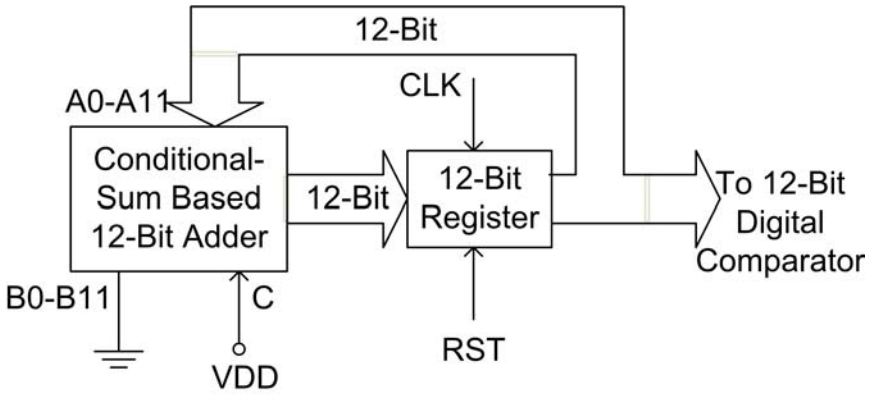


Figure 3.14: Architecture of the 12-Bit High-Speed Counter

The 12-bit high-speed counter consists of two blocks; the conditional-sum based 12-bit adder and the 12-bit register. The 12-bit register can be implemented by basic digital design technique using D flip flops. CLK and RST are the inputs connected to the 12-bit register. A0 – A11, B0 – B11, and C (carry-in) are the inputs to the 12-bit conditional sum-based adder. The 12-bit digital data is the output from the block. To function as an incrementer, the inputs B0 – B11 are connected to ground and C (carry) is connected to supply voltage (VDD). The RST input is connected to the reset circuit output and the 12-bit output of the incrementer is connected to the input of the 12-bit register. The Output of the register is used as the 12-bit counter output as well as the input (A0 – A11) to the incrementer. The CLK input is connected to the output of the clock driver.

3.6.2 Implementation

The top level hierarchical blocks of the 12-Bit high-speed counter is shown in Figure 3.15.

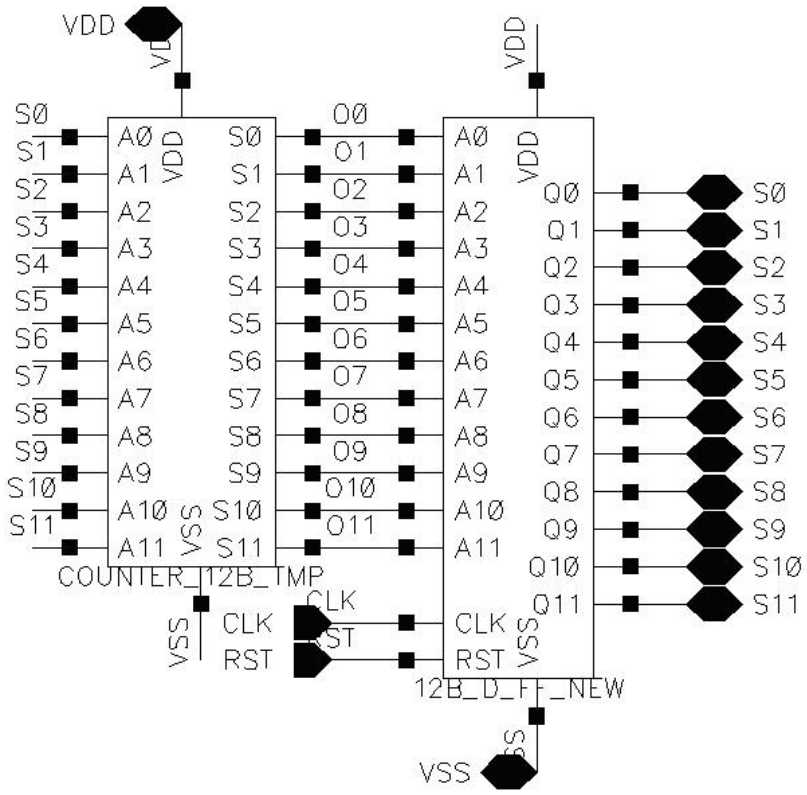


Figure 3.15: Implementation of the Top-level Hierarchical Blocks of the 12-Bit High-Speed Counter. The two shown blocks are 12-Bit Incrementer and 12-Bit Register

Only one set of inputs of the adder (A0 – A11) is available for external connection. The other set of inputs (B0 – B11) and the carry input are internally connected to ground and VDD respectively. The outputs of the 12-bit incrementer (O0 – O11) are connected to the input of 12-bit register. The outputs of the register (S0 – S11) serve as the output from the 12-bit counter block and the input (A0 – A11) to the incrementer.

The whole structure of the adder is changed to work as an incrementer. The previous structure of the adder was implemented using 2-to-1 multiplexers only [42]. The modified structure is not implemented using 2-to-1 multiplexers only, as shown in Figure 3.16.

The implementation of the proposed 12-Bit incrementer is shown in Figure 3.16.

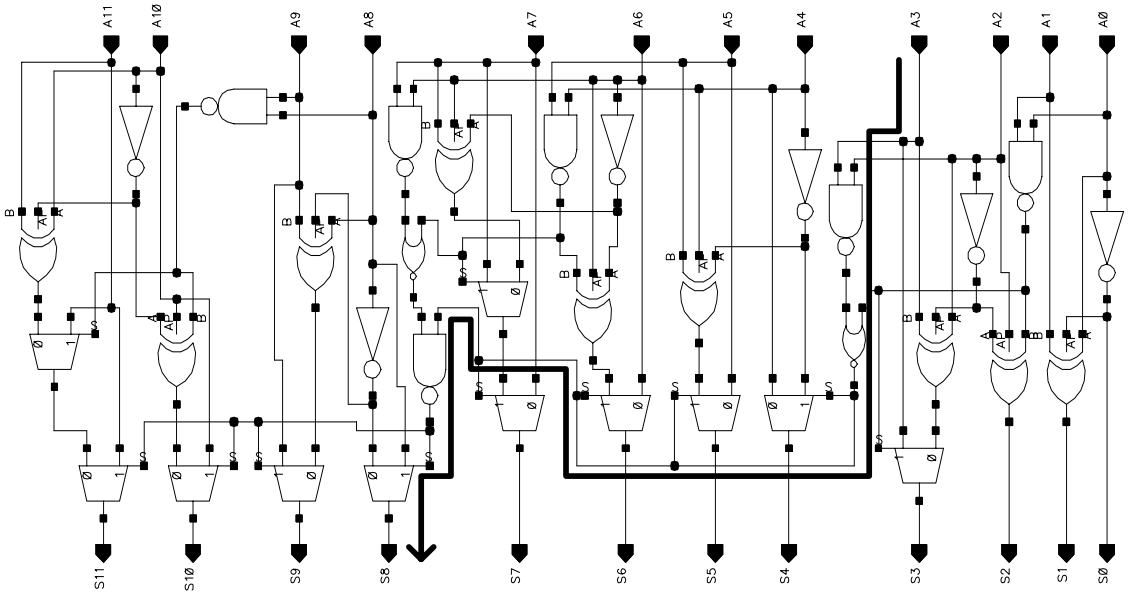


Figure 3.16: Implementation of the 12-Bit High-Speed Incrementer

From Figure 3.16, the gates used in the design of the 12-bit incrementer are:

- 2 NOR
- 6 NAND
- 11 2-to-1 MUX (multiplexer)
- 9 Simplified XOR (Exclusive-OR), and
- 6 INVERTER

The transistor widths of all the NMOS and PMOS in incrementer implementation are 2.5 μm and 5 μm respectively. The same transistor widths are used to implement the 12-bit register.

The critical path delay for the proposed incrementer is denoted by thick black line in Figure 3.16 which consists of two NAND, one NOR and one 2-to-1 MUX. This is the lowest critical path delay achieved by any incrementer design. Therefore, the critical path delay for the design is,

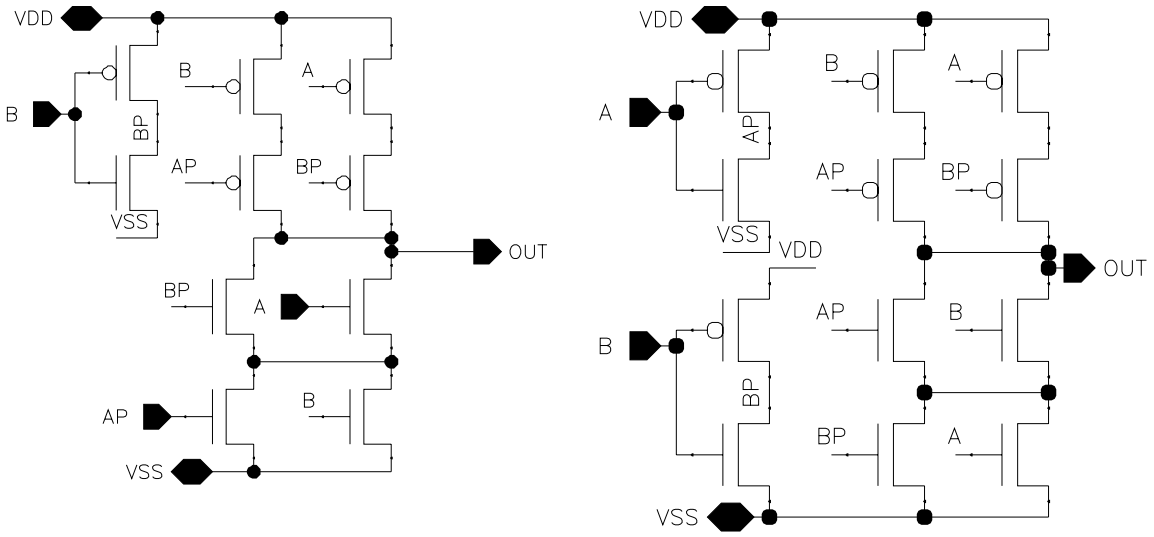
$$2 \bullet t_{NAND} + t_{NOR} + t_{MUX} \tag{3.4}$$

Where, t_{NAND} and t_{NOR} are propagation delay of NAND and NOR gates respectively

Now, for the proposed design, total logic gates required are,

$$\text{2-NOR + 6-NAND + 11-MUX + 9-Sim. XOR + 6-INV} \tag{3.5}$$

All the gates used in the incrementer design are basic logic gates except the simplified-XOR gate. The difference between the simplified-XOR and XOR gate can be easily understood from Figure 3.17. The simplified-XOR uses one less inverter than the regular XOR. Hence, the simplified-XOR requires three inputs.



(a) Simplified-XOR Gate (b) XOR Gate

Figure 3.17: Implementations of (a) Simplified XOR and (b) XOR

3.6.3 Simulation Results

The simulation waveform for all the outputs from Bit 0 to Bit 11 of the 12-bit high-speed counter is shown in Figure 3.18.

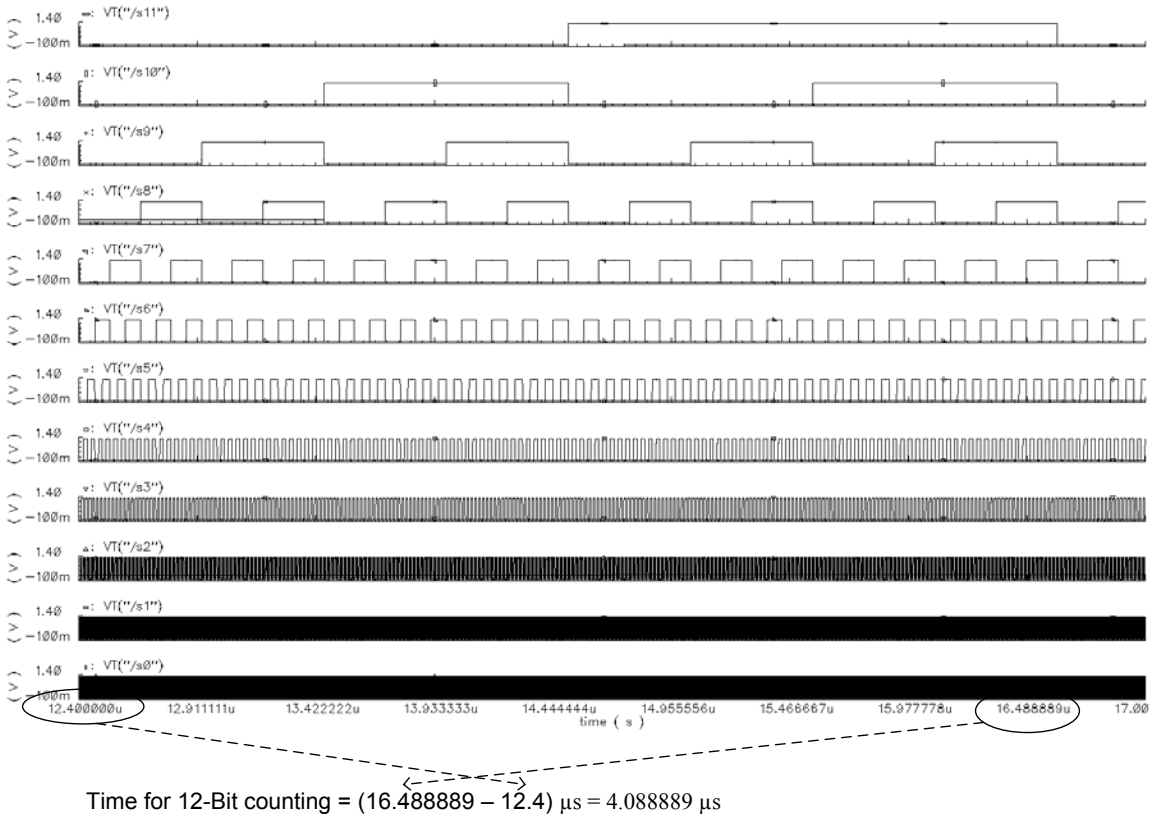


Figure 3.18: Simulation Waveforms for the 12-Bit High-Speed Counter

As shown in the simulation waveforms of Figure 3.18, the 12-bit high-speed counter is counting efficiently without any glitches or without missing any count at 1 GHz clock. Furthermore, the time taken for full cycle of 12-bit counting is also calculated in Figure 3.18 which is equal to 4.088889 µs. Therefore, the frequency of operation for one cycle is 244 KHz for the 12-bit counter. The full voltage swing for all the bits is achieved. Hence, the functionality and the accuracy of the counter are correct.

3.7 12-Bit Digital Comparator

The 12-bit digital comparator is the decision block to generate PWM pulses with accurate duty cycle. The digital comparator compares digital data in the 12-bit data register with the 12-bit counter value. The output of the comparator goes low when both data are equal and it remains high for all other conditions. Hence, the pulse-width of the output low pulse is equal to 1 ns only.

3.7.1 Architecture

The architecture of the 12-bit digital comparator is shown in Figure 3.19.

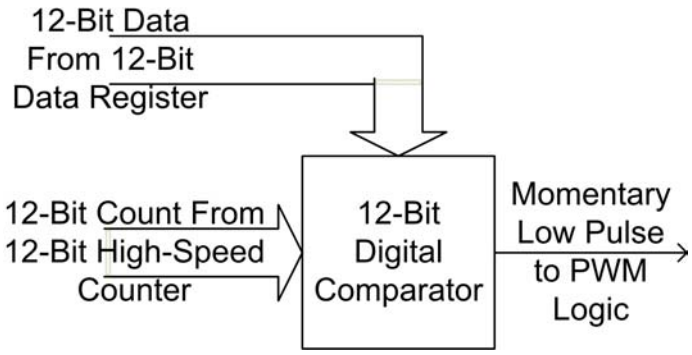


Figure 3.19: Architecture of the 12-Bit Digital Comparator

The digital comparator has two 12-bit inputs, one is connected to the 12-bit data register and another is connected to the output of the counter. The comparator output is connected to the PWM logic block.

3.7.2 Implementation

The implementation of the 12-Bit digital comparator is shown in Figure 3.20.

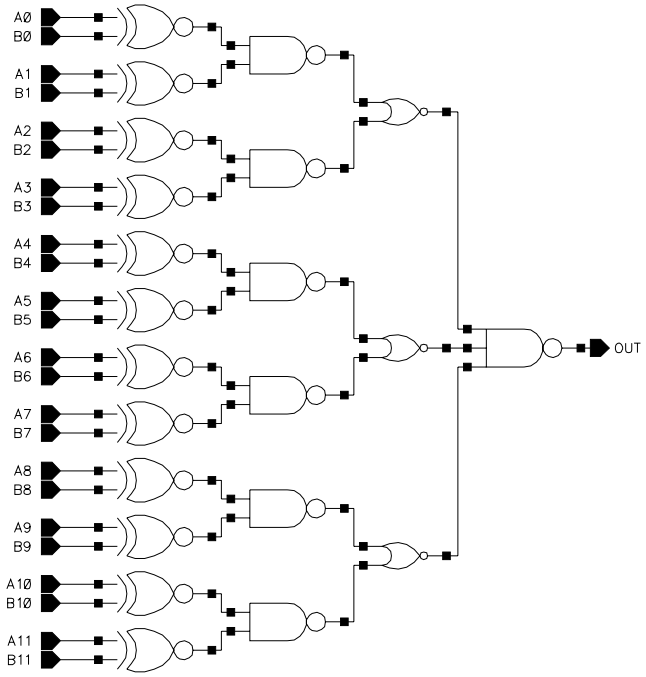


Figure 3.20: Implementation of the 12-Bit Digital Comparator

As shown in Figure 3.20, the 12-bit digital comparator is designed using twelve XNOR, six 2-input NAND, three NOR and one 3-input NAND gates. The minimum possible transistor-widths for all the logic gates are used.

The twelve XNOR gates, one for comparing each bit, are used to decide whether the inputs are equal or not. The single bit logical value for 12-bit comparison can be obtained by logical AND operation of the twelve bits. The twelve input AND gate is the simplest implementation. But, high fan-in to any gate results in larger delay and area. Hence, to avoid the large fan-in problem, multiple stages of the AND gate is used. To further simplify the circuit for efficient CMOS implementation, the multiple stages of the AND gate is replaced with multiple stages of 2-input NAND, NOR and 3-input NAND gates. The number of transistors in 2-input NAND and 2-input NOR are four. On the other hand, the transistor count for 2-input AND is six. Hence, the number of transistors used in NAND, NOR and NAND implementation are lower than the AND based implementation.

3.7.3 Simulation Results

The simulation waveform of the 12-Bit digital comparator is shown in Figure 3.21.

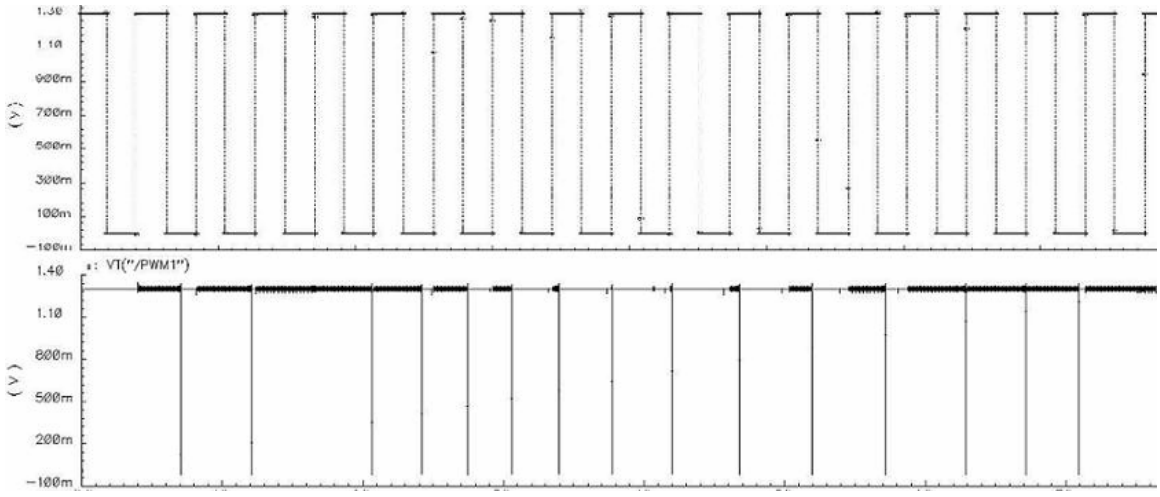


Figure 3.21: Simulation Waveforms for Output of the 12-Bit Digital Comparator

The upper waveform in Figure 3.21 shows 244 KHz clock signal and the lower waveform shows the output of the 12-bit digital comparator for 20 KHz frequency. The

pulse has full voltage swing. The change in the duty cycle is seen from the simulation waveform. Hence, the correct functionality of the 12-bit digital comparator is achieved.

3.8 PWM Logic

The PWM logic is designed to latch the momentary low pulse generated by the 12-Bit digital comparator and the reset pulse received from the reset circuit. The momentary low pulse is latched logic low until the reset pulse is received. Similarly, the reset pulse is latched logic high until next momentary low pulse is received. Hence, the output generated is the desired PWM pulses. The output is also used as enable signal to the clock driver block.

3.8.1 Architecture

The architecture of the PWM logic is shown in Figure 3.22.

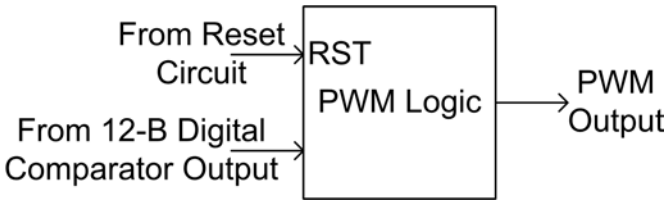


Figure 3.22: Architecture of the PWM Logic

The PWM logic has two inputs, first is the RST (reset) which is connected to the output of the reset circuit and second is the CLK which is connected to the output of the 12-bit digital comparator. The RST input is a momentary low pulse and the CLK input is a momentary high pulse. The PWM logic latches one of the two pulses until the other is received. The generated output is the PWM pulse of the desired duty cycle. The output is connected to the class – D output stage of the class – D output stage, filter and control section and to the enable input of the clock driver.

3.8.2 Implementation

The implementation of the PWM logic block is shown in Figure 3.23.

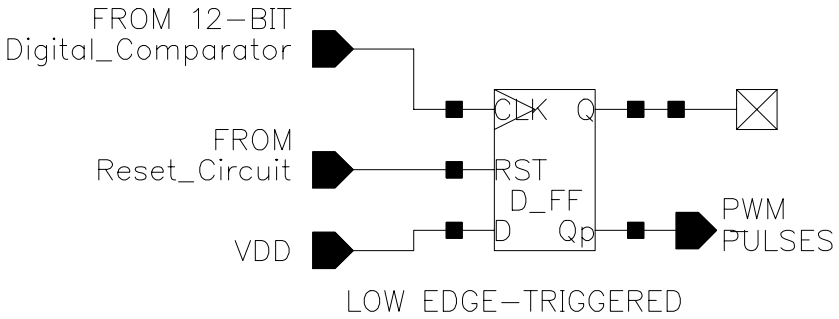


Figure 3.23: Implementation of the PWM Logic

The PWM logic is implemented using falling edge-triggered D-Flip-Flop. The modifications in the PWM logic for desired functionality are described below.

First, D input of the flip-flop is connected to supply (VDD). Q' is used as the output instead of Q. Q can be used as inverted PWM pulses output. The CLK input of the flip-flop is connected to the output of the 12-bit digital comparator and the RST input is connected to the output of the reset circuit. The operation of the PWM logic is explained below.

When falling edge at the CLK input (output of the 12-bit digital comparator) is detected, the logic level at D (VDD) is latched at Q output and inverted logic level of D is latched at Q' output. Briefly, at falling edge of the momentary low pulse, Q goes logic high and Q' goes logic low. Furthermore, when the RST input (output of the reset circuit) goes high, Q output falls logic low and Q' output goes logic high. Hence, full swing and accurate duty cycle of the PWM pulses are achieved at the output of the PWM logic block.

The transistor level implementation of the PWM logic is shown in Figure 3.24.

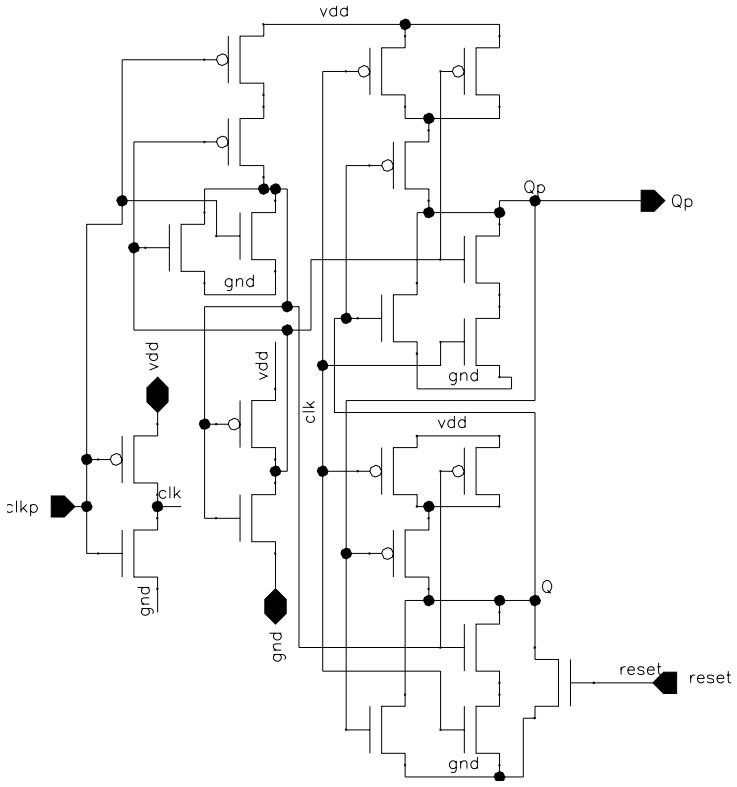


Figure 3.24: Transistor Level Implementation of the PWM Logic

The transistor widths of all NMOS and PMOS are minimum possible for CMOS logic. The implementation is simplified for the fixed inputs.

3.8.3 Simulation Results

The simulation waveforms for the inputs and output of the PWM logic with 244 KHz clock is shown in Figure 3.25.

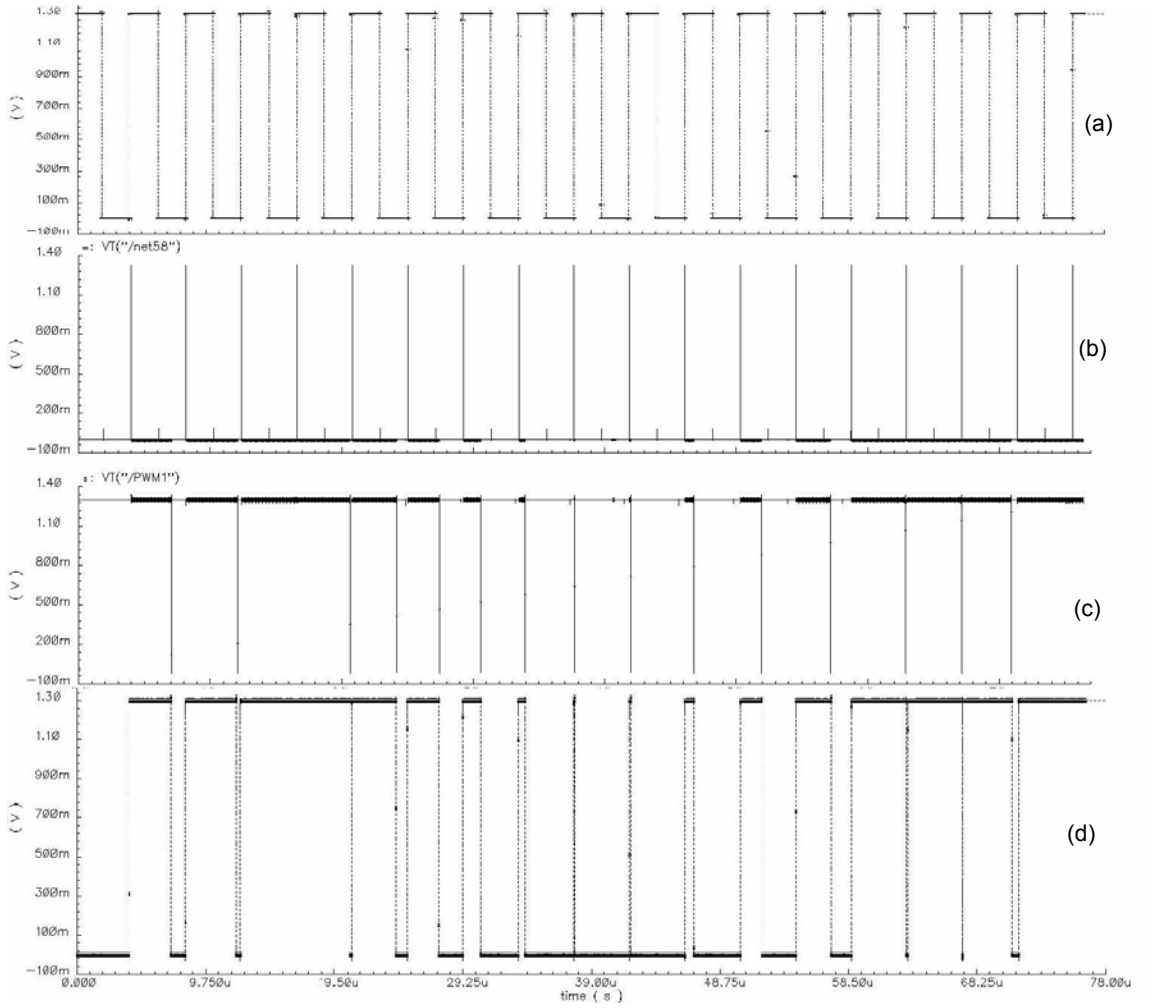


Figure 3.25: Simulation Waveforms for (a) 244 KHz Clock, (b) Output of the Reset Circuit (Input at RST), (c) Output of the 12-Bit Digital Comparator (Input at CLK) and (d) Output of the PWM Logic

Figure 3.25 (a) shows 244 KHz clock which is used as a reference to other waveforms. Figure 3.25 (b) shows the output of the reset circuit which is connected at the RST input of the PWM logic. Figure 3.25 (c) shows the output of the 12-bit high-speed comparator which is connected at the CLK input of the PWM logic. And finally, in Figure 3.25 (d) the PWM pulses generated at the output of the PWM logic is shown.

From Figure 3.25, the accuracy of the PWM pulses generated by the PWM logic and hence the digital pulse-width modulator section is shown. The correct functionality of the PWM logic is understood from Figure 3.25(b) - Figure 3.25(d). The full voltage swing without any glitches and inaccuracy is achieved. The pulses with very short duration are also present which shows accurate 12-bit resolution.

3.9 Summary

First, we explained the operation of the digital pulse-width modulator section. The main blocks described in this chapter are clock generator, clock driver, reset circuit, 12-bit high-speed counter, 12-bit digital comparator and PWM logic. All blocks are explained by dividing them in three parts namely, architecture, implementation and simulation results. In architecture, basic operation and input – output were described. Transistor and/or gate level implementations were described with appropriate details in the implementation part of each block. And finally, the simulation results obtained by the measurement and/or the waveforms were presented for authenticity of the logical operation of all the blocks.

Chapter 4

Design of Class – D Output Stage, Control and Filter

4.1 Introduction

In this chapter, the class – D output stage, control and filter section of the device for hearing-testing will be discussed. First, operation and main design concerns for this section will be described. The detailed explanation of the control system will also be described. The architecture, implementation and simulation results of the class – D output stage, the control and the filter section will be presented

4.2 Operation and Main Design Concerns of the Class – D Output Stage, Control and Filter Section

The class – D output stage, control and filter section is the second and final section of the device for hearing-testing. The architecture of this section is shown in Figure 4.1.

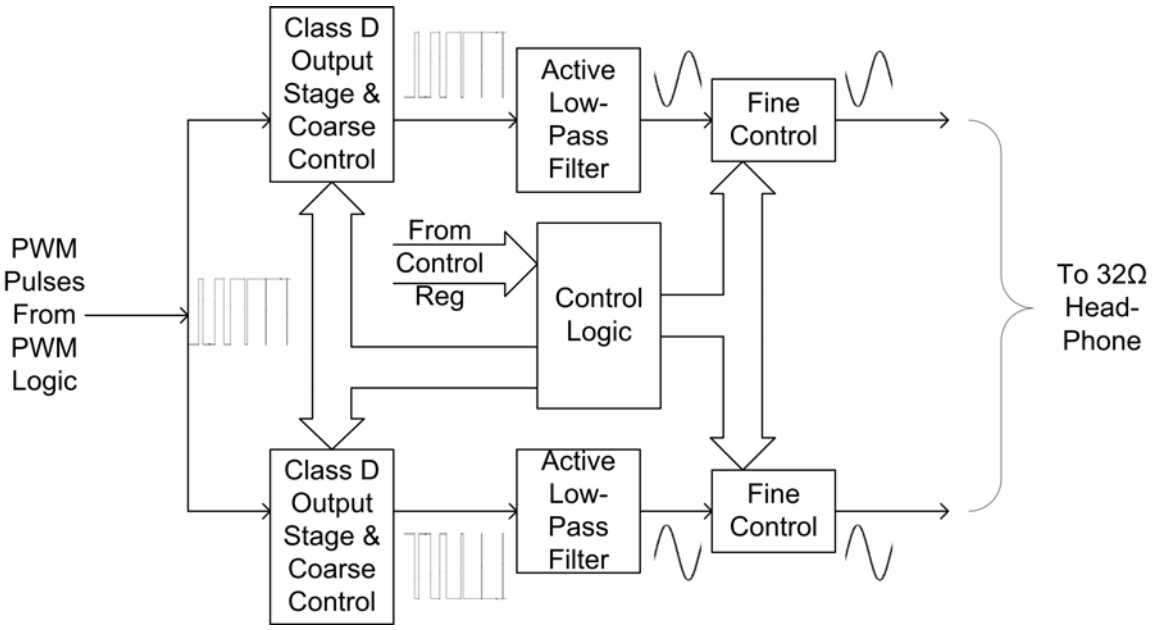


Figure 4.1: Architecture of the Class-D Output Stage, Control and Filter Section

As shown in Figure 4.1, the first input to this section is the PWM pulses generated by the digital pulse-width modulator section and the other input is fed from the 7-bit control register. The output from this section is the controlled sound waves with desired SPL which is fed to 32 Ω head-phones. To generate fully differential sound waves at the output, the H-bridge design [26], [47], [48] is chosen for class – D output stage, active low-pass filter and control blocks.

The main blocks of this section are the control logic, the class – D output stage and coarse control, the active low-pass filter and the fine control. The operation of this device-section is explained below.

This section starts functioning when the reset pulse goes high and the 7-bit control value is loaded in the control logic block. The control logic configures the coarse and fine control blocks according to the control value. When the PWM pulses are fed into this section from the digital pulse-width modulator, the PWM pulses are divided into two branches of mutually inverted PWM pulses. These mutually inverted PWM pulses are coarsely controlled by the class – D output stage and coarse control block. These coarsely controlled PWM pulses are converted into sinusoidal sound waves by the active low-pass filter. The sinusoidal sound waves have mutual phase difference of 180^0. Finally, these sound waves are finely tuned by the fine control block to achieve

accurately controlled sound waves across the output. The class-D output stage and coarse control block and the fine control block are explained in detail in sections 4.4 and 4.6 respectively. The main design considerations for this section are discussed in the following paragraphs.

By using the H-bridge, we are able to generate fully differential sinusoidal waves across the output. The advantage is that a 2.6 V peak-to-peak signal can be generated using single 1.3 V power supply. Hence, four times larger power can be generated without using any supply multipliers or other complex design techniques.

Another concern is the selection of the cut-off frequency for the active low pass filter. Generally, at the cut-off frequency, the gain should be around -3 dB. For the proposed design, if the cut-off frequency is chosen near 20 KHz, the SPL for 20 KHz frequency will be 6 dB less than the SPL at lower frequencies. Hence, the accuracy of the control for the full range of 20 Hz to 20 KHz is susceptible. Therefore, the cut-off frequency should be chosen such that the loss in SPL at 20 KHz won't exceed ± 0.5 dB SPL. Hence, we have chosen the cut-off frequency for the active low-pass filter as 100 KHz and the chosen sampling frequency is 244 KHz. Another important parameter for the output sound waves is the total harmonic distortion (THD). The total harmonic distortion can be controlled by the low-pass filter. To reduce the higher frequency distortion from the desired sound waves, we need to filter out the higher frequency components efficiently. Instead of the first-order low-pass filter, second-order low-pass filter is chosen to remove high-frequency components more efficiently. Hence, 2^{nd} order, non-inverting, dual-feedback configuration of the Butterworth filter is used to implement the active low-pass filter.

As the control block is an important component of the design, the basics of the control design are explained in the following sub-section.

4.2.1 The Fundamentals of the Control Design

Usually, the dB SPL unit is used to measure the hearing-ability. The range of the SPL output was intended from 0 to 113 dB SPL. From Equation 4.1, 113 dB SPL can be achieved by 20 mW R.M.S. (root-mean-square) power. This range can be covered using 7-bit binary value. Hence, 7-bit length of the control register is chosen. The content of

the 7-bit control register is updated by PC using USB connection on every rising edge of 244 KHz clock frequency (reset pulse).

The sound pressure level (SPL) in dB can be calculated using Equation (4.1).

$$SPL(in \quad dB) = 10\log_{10}(\frac{P_{actual}}{P_{reference}}) \tag{4.1}$$

Where, P_{actual} is actual R.M.S. power applied to head-phones in Watts, and

$P_{reference}$ is R.M.S. power of surrounding environment in Watts [49].

R.M.S. power can be calculated using RMS or peak-to-peak voltages.

Power applied to head-phones is,

$$P_{actual} = \frac{V_{RMS}^2}{R} = \frac{V_{P-P}^2}{8 \cdot R} \tag{4.2}$$

Where, R is load (head-phone) resistance which is equal to 32 Ω for our design. Therefore, the Equation – 4.2 can be simplified to,

$$P_{actual} = \frac{V_{P-P}^2}{8 \times 32} = \frac{V_{P-P}^2}{256} \tag{4.3}$$

The head-phones used for the proposed hearing-testing device have a sensitivity of 100 dB SPL. The sensitivity of head-phones is measured as dB SPL generated at 1 mW R.M.S. input. Hence, for 1 mW power applied to the head-phones, 100 dB SPL output is generated. Replacing these values in Equation 4.1, we can calculate reference power for our head-phones which is equal to 10^{-13} W as shown in Equation 4.4.

$$100 = 10\log_{10}(\frac{1 \times 10^{-3}}{P_{reference}})$$

$$\therefore 10 = \log_{10}(\frac{1\times10^{-3}}{P_{reference}})$$

$$\therefore 10^{10} = \frac{1\times10^{-3}}{P_{reference}}$$

$$\therefore P_{reference} = 10^{-13} \tag{4.4}$$

By replacing Equation 4.3 and Equation 4.4 in Equation 4.1, the equation to calculate dB SPL from peak-to-peak voltage:

$$SPL(in \quad dB) = 10\log_{10}(\frac{V_{P-P}^2}{256\times10^{-13}}) \tag{4.5}$$

Equation 4.5 can be rewritten as,

$$V_{P-P} = \sqrt{256\times10^{(0.1\bullet SPL-13)}} \tag{4.6}$$

The values of $V_{P\text{-}P}$ (peak-to-peak voltage) for sound pressure level from 0 to 127 dB can be calculated using Equation 4.6. The plot for calculated $V_{P\text{-}P}$ for input SPL is shown in Figure 4.2.

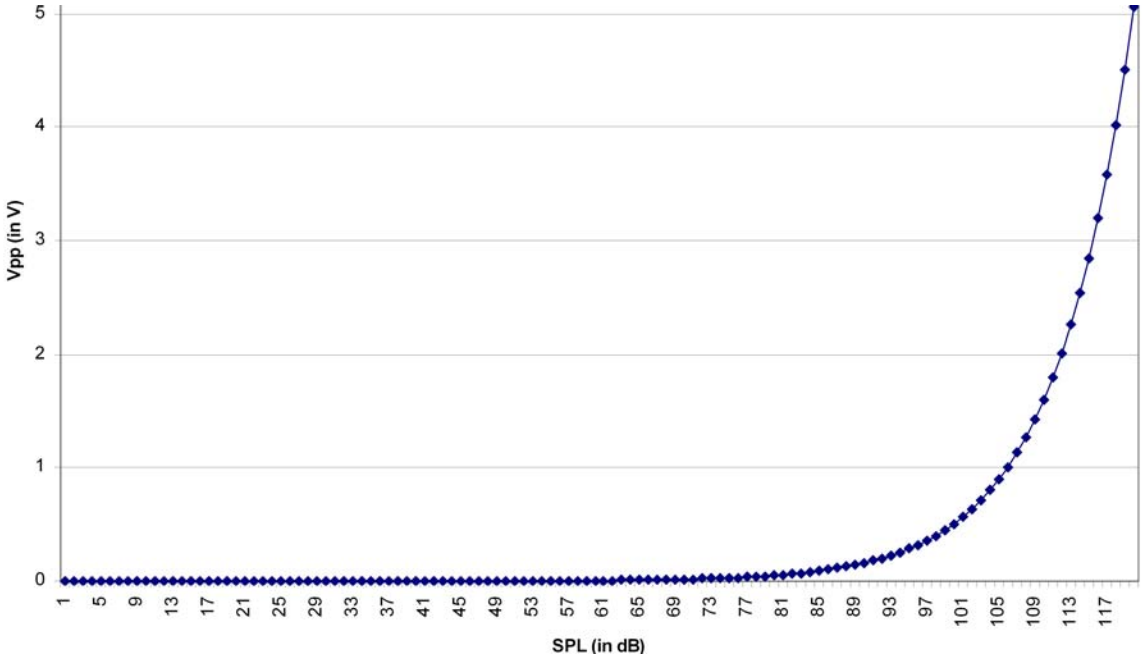


Figure 4.2: Peak-To-Peak Voltage Across Headphone Vs. SPL (Sound Pressure Level in dB)

As shown in Figure 4.2, the plot of peak-to-peak voltage with respect to SPL (in dB) is exponential. The lowest peak-to-peak voltage step from 1 to 2 dB SPL is 0.693 μV. The peak-to-peak voltage for 1 dB SPL is 5.68 μV. On the other hand, the highest peak-to-peak voltage step from 112 to 113 dB SPL is 0.25 V and the peak-to-peak voltage at 113 dB SPL is 2.26 V. It is a challenge to design control step from 0.69 μV to 0.25 V. The range of peak-to-peak voltage is also very large from 5.68 μV to 2.26 V. The bit resolution required for accurate control, can be calculated as,

$$Maximum \quad Count = \frac{2.26}{\min.\ \ step} = \frac{2.26}{0.692669 \times 10^{-6}} = 3262742$$

$$\therefore 2^x \geq 3262742$$

$$\therefore x \log_{10} 2 \geq \log_{10} 3262742$$

$$\therefore x \geq \frac{\log_{10} 3262742}{\log_{10} 2}$$

$$\therefore x \geq 21.64$$

$$\therefore x = 22$$

The simpler control can be designed using 22-bit implementation. But, for the input range from 0 to 113 dB SPL, only 7-bits are required. Hence, we used curve-fitting technique to achieve 22-bit equivalent control using 7-bits. The full SPL range from 0 to 127 is divided into 16 sections of 8 steps each. Each of these sections has consecutively increasing slope. Each of the 16 sections is selected by unique combination of four most significant bits of the control register. Furthermore, the 8 steps of each section are selected by a unique combination of the three least significant bits. Hence, the whole system can be controlled by only 7-bits.

The control is divided into coarse and fine control sections. The coarse control controls the top 5 sections among the total 16 sections. On the other hand, the fine control controls the remaining 11 sections. The 8 steps of all the sections are controlled by the fine control block. The selection of the sections and steps depends on the binary value of 7-bit control register. The appropriate selection logic for sections and steps is designed using the control logic block. The coarse control is designed using digital

design techniques and the fine control is designed using digitally controlled analog design technique (based on active device), based resistor network using CMOS transmission-gates (TG)).

The main blocks of the class – D output stage, control and filter section are discussed in the following sections.

4.3 Control Logic

The control logic is designed to generate signals for switch selection for the coarse and fine controls. Furthermore, it also generates digital outputs equivalent to 22-bit resolution from 7-bit control value. The selection switches in the coarse and fine controls are designed using CMOS transmission-gates (TG). The control logic selects different combination of switches depending upon the 7-bit control register value. In the class – D output stage & coarse control block, only one of the five switches is selected. Similarly, depending upon the required section and steps, only one combination of 3-bits is selected for fine control.

4.3.1 Architecture

The architecture of the control logic is shown in Figure 4.3.

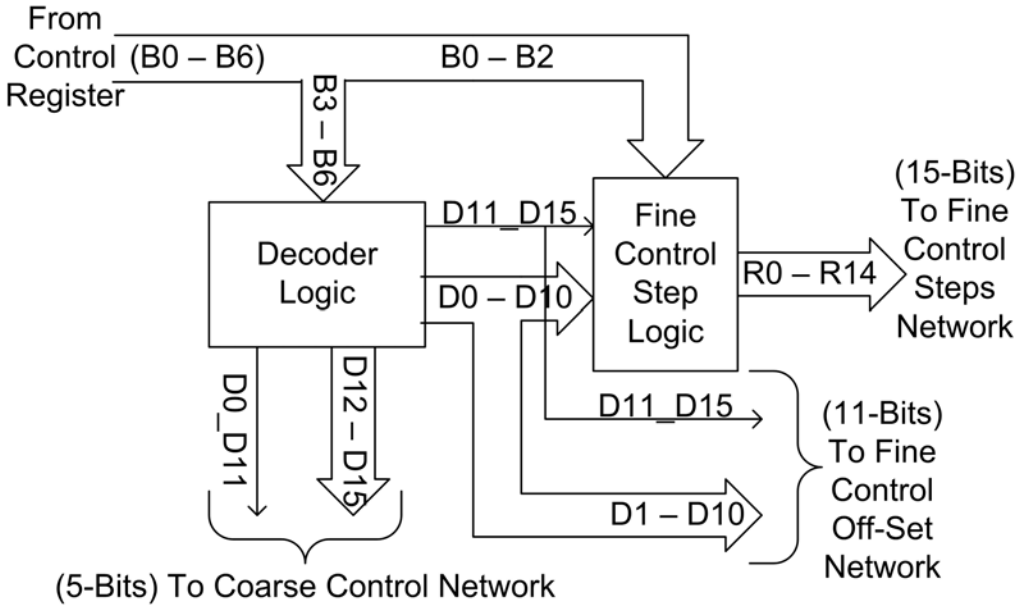


Figure 4.3: Architecture of the Control Logic

There are two main blocks of the control logic, the decoder logic and the fine control step logic. The 7-bit control value is the only input to the control logic. The control logic generates 5-bit output to the class – D output stage and coarse control block, 15-bit output to the fine control steps network and 11-bit output for the fine control off-set network. Hence, 31-bit output is generated from 7-bit input to achieve 22-bit accurate resolution.

The decoder logic generates 18 decoded outputs from the four most-significant bits of the 7-bit control register. Among these 18 outputs, 16 outputs, D0 to D15, are decoded outputs which represent unique combination of input four bits. The other two, D0_D11 and D11_D15 outputs are logical AND of D0 to D11 and D11 to D15 respectively. The output D0_D11 is used in the coarse control block and the output D11_D15 is used in the fine control block only. The coarse control block is actively controlling the output SPL for control value from 96 to 127. On the other hand, the fine control block is actively controlling the output SPL for 7-bit control register value from 0 to 95. The fine control block is divided into two parts namely, offset and control steps which are explained in section 4.6. The outputs D1 to D10 and D11_D15 (11-bits) are fed to the off-set network of the fine control.

The fine control step logic is designed to generate digital signals to select appropriate group of 8 steps with different slopes. The slope of the group depends on the decoder inputs to this block and hence the selected section among the 16 sections. Fifteen parallel branches of transmission-gate (TG) network are used in the fine control steps network. The inputs to the fine control steps network are D0 to D10, D11_D15 and three least-significant bits of the control value. The outputs generated are R0 to R14 (15 bits) to the steps control block of the fine control.

4.3.2 Implementation

The implementation of the top level hierarchical blocks of the control logic is shown in Figure 4.4.

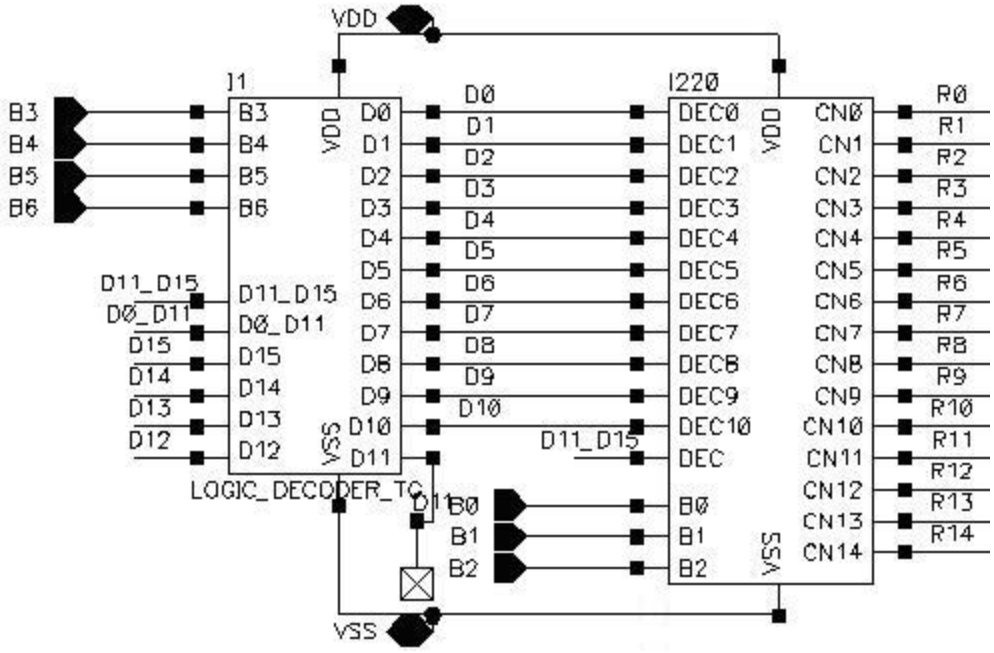


Figure 4.4: Implementation of Top Level Hierarchical Blocks of the Control Logic

In Figure 4.4, the top-level hierarchical blocks of the decoder logic and the fine control step logic with their inputs and outputs are shown. 7-bit input from the control register is shown as B0 to B6. The outputs to different blocks are shown as D0-D15, D0_D11, D11_D15 and R0 to R14. The decoder output D11 is not connected anywhere because it is used internally to generate outputs D0_D11 and D11_D15. The individual implementation of both blocks is presented in the following paragraphs.

The implementation of the decoder logic block is shown in Figure 4.5.

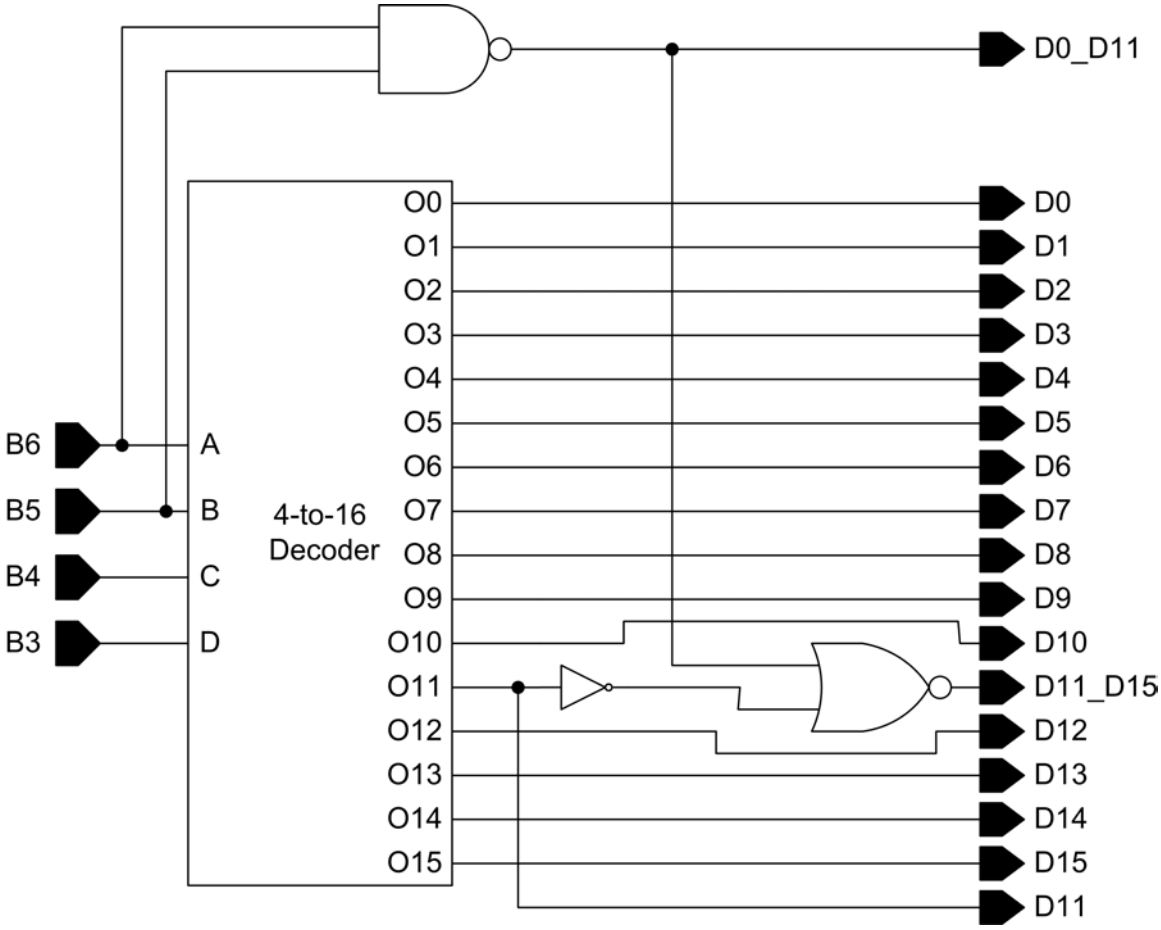


Figure 4.5: Implementation of the Decoder Logic

The decoder logic block is implemented using one 4-to-16 decoder, one NAND gate, one NOR gate and one inverter. The 4-to-16 decoder, designed using basic digital design techniques, generates D0 to D15 outputs. The additional signals, D0_D11 and D11_D15, are generated by one NAND, one NOR and one inverter instead of multiple stages of AND gates. All the NMOS and PMOS transistors are implemented using minimum widths.

The optimization to generate D0_D11 and D11_D15 is explained now. The logical equation for D0_D11 can be described as,

$$D0\_D11 = D0 \bullet D1 \bullet D2 \bullet D3 \bullet D4 \bullet D5 \bullet D6 \bullet D7 \bullet D8 \bullet D9 \bullet D10 \bullet D11 \quad (4.7)$$

From Equation 4.7, D12 to D15 are excluded from this logic because only one

among 16 outputs of 4-to-16 decoder is enabled at any time. Therefore, D0_D11 can be rewritten as,

$$D0\_D11 = (D12 + D13 + D14 + D15)' \tag{4.8}$$

D12 to D15 are the most significant four bits of 4-to-16 decoder output. These four bits can also be represented by logic '1' at B5 and B6. Therefore, Equation 4.8 can be further simplified as,

$$D0\_D11 = (B5 \bullet B6)' \tag{4.9}$$

So, Instead of logical AND of inputs D0 to D11, we use logical NAND of B5 and B6 inputs which resulted in reduced area and time-delay.

Similarly, D11_D15 signal is described as,

$$D11\_D15 = D11 \bullet D12 \bullet D13 \bullet D14 \bullet D15 \tag{4.10}$$

Logical AND of D12 – D15 can be represented by inverted D0_D11.

$$\begin{aligned} D11\_D15 &= D11 \bullet (D12 \bullet D13 \bullet D14 \bullet D15) \\ D11\_D15 &= D11 \bullet (D0\_D11)' \\ D11\_D15 &= (D11' + D0\_D11)' \end{aligned} \tag{4.11}$$

Therefore, D11_D15 can be implemented using one inverter and one NOR gate.

By combining all these blocks, we designed the decoder logic block as shown in Figure 4.5.

The second block of the control logic is the fine control step logic. This block is designed to provide signals for selecting a group of 3-bit steps in the fine control block. The implementation of the fine control step logic is shown in Figure 4.6.

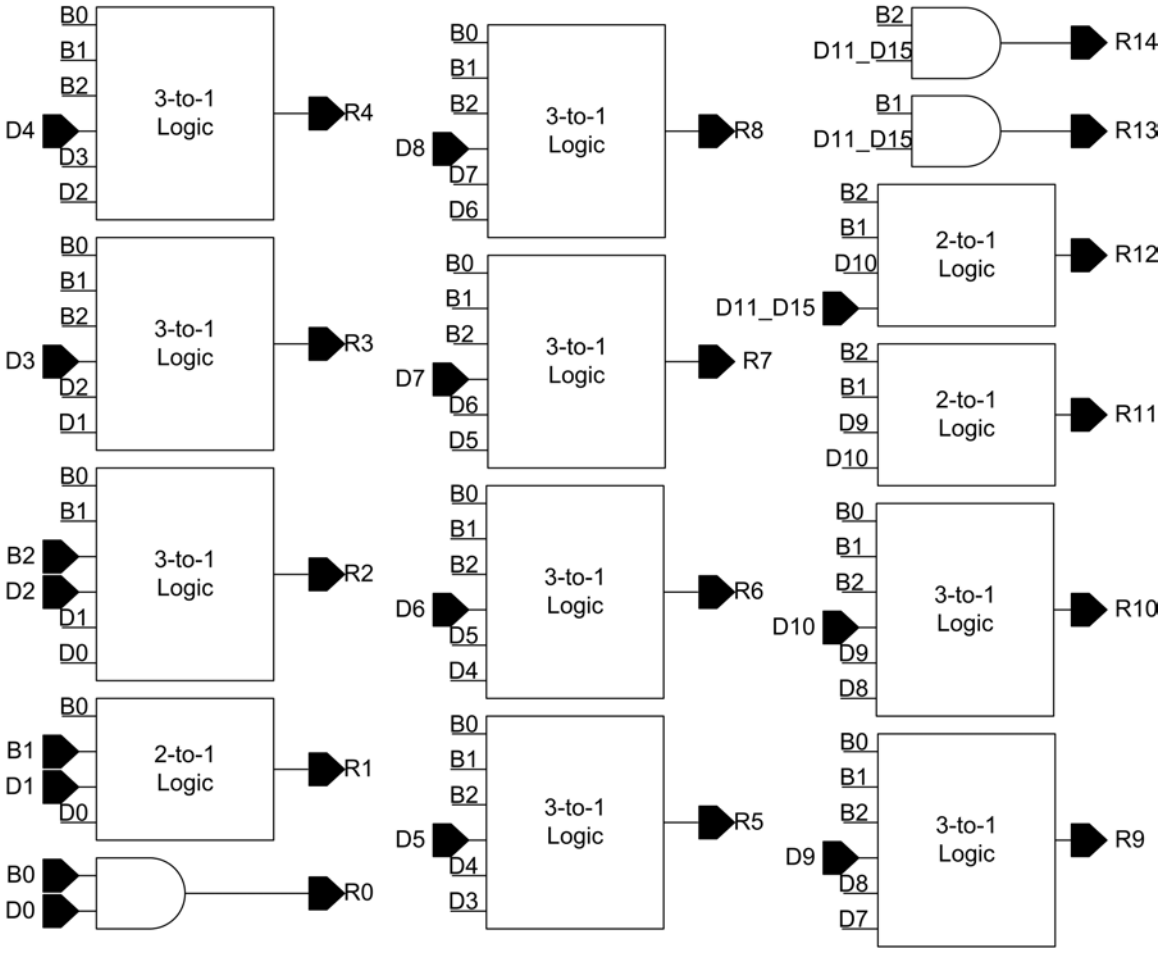


Figure 4.6: Implementation of the Fine Control Step Logic

The fine control step logic is designed using three AND gates, three 2-to-1 logic blocks and nine 3-to-1 logic blocks. The inputs to the fine control step logic are B0 – B2 (three least significant bits of the control register), D0 to D10 and D11_D15 (decoder logic outputs). The R0 to R14 outputs are generated to select the appropriate TG network in the fine control steps network. The group of three bit outputs is different for each decoder input. For example, for D0 input, the group of 3-bit outputs is R0, R1 and R2. However, for D1 input, the group of 3-bit outputs is R1, R2 and R3. For the second case, the increment step is double than the first case. Hence, different slopes for different sections (decoder input) are achieved.

The implementation of the 2-to-1 logic block and the 3-to-1 logic block is shown in Figure 4.7.

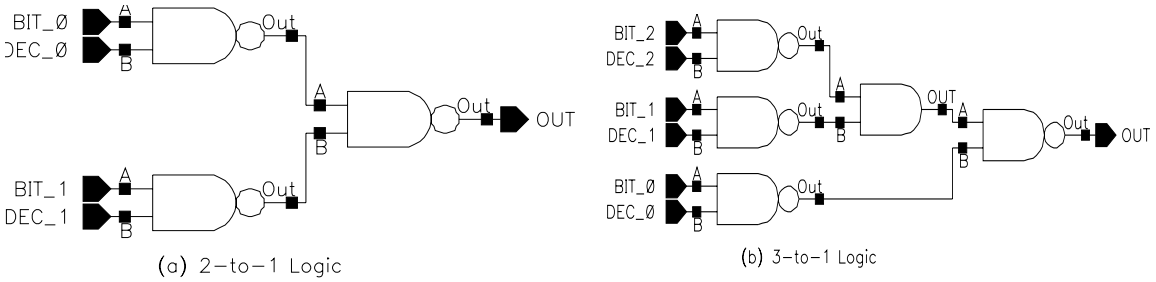


Figure 4.7: Implementation of (a) 2-to-1 Logic and (b) 3-to-1 Logic

The 2-to-1 logic block is implemented using three NAND gates and the 3-to-1 logic block is implemented using four NAND and one AND gates. The logical functions performed in both the blocks can be expressed as:

In 2-to-1 block (From Figure 4.7 (a)),

$$OUT = ((BIT\_0 \bullet DEC\_0)' \bullet (BIT\_1 \bullet DEC\_1)')'$$
$$\therefore OUT = (BIT\_0 \bullet DEC\_0) + (BIT\_1 \bullet DEC\_1) \quad (4.12)$$

In 3-to-1 block (From Figure 4.7 (b)),

$$OUT = ((BIT\_0 \bullet DEC\_0)' \bullet ((BIT\_1 \bullet DEC\_1)' \bullet (BIT\_2 \bullet DEC\_2)'))'$$
$$\therefore OUT = ((BIT\_0 \bullet DEC\_0)' \bullet ((BIT\_1 \bullet DEC\_1) + (BIT\_2 \bullet DEC\_2))')$$
$$\therefore OUT = (BIT\_0 \bullet DEC\_0) + (BIT\_1 \bullet DEC\_1) + (BIT\_2 \bullet DEC\_2) \quad (4.13)$$

From Equation 4.13, each output is selected for three sections which are implemented using 3-to-1 logic. For example, an output is selected for sections 0, 1 and 2. For section 0, the output is selected when B0 (LSB of the control register) is high. For section 1, the output is selected when B1 is high and for section 2, the output is selected when B2 is high. Hence, the single output is used for three different slopes (different sections). Similarly, from Equation 4.12, the output of 2-to-1 logic is used for two different slopes of different sections and the output of the AND gate is used for one slope of only one section.

4.3.3 Simulation Results

The simulation waveforms for all thirty-one outputs were generated to check the functionality of the control logic block. The simulation waveforms represent correct logic operation of the control logic block. The simulation waveforms of individual blocks proved correct logic and desired speed.

4.4 Class – D output stage & Coarse Control

The coarse control is implemented using parallel current amplifiers. Generally, the class – D output stage is used to supply sufficient current to the load. Hence, the class – D output stage and the coarse control are combined together for output control.

The coarse control is designed to divide over-all control design in larger steps by supplying different amount of current. The peak-to-peak voltage steps offered by the coarse control are 0.4 V, 0.64 V, 1.0 V, 1.6 V and 2.26 V. For the control value from 0 to 95, 96 to 103, 104 to 111, 112 to 119 and 120 to 127, the peak to peak voltage steps selected respectively are 0.4 V, 0.64 V, 1.0 V, 1.6 V and 2.26 V.

4.4.1 Architecture

The architecture of the class – D output stage and coarse control block is shown in Figure 4.8.

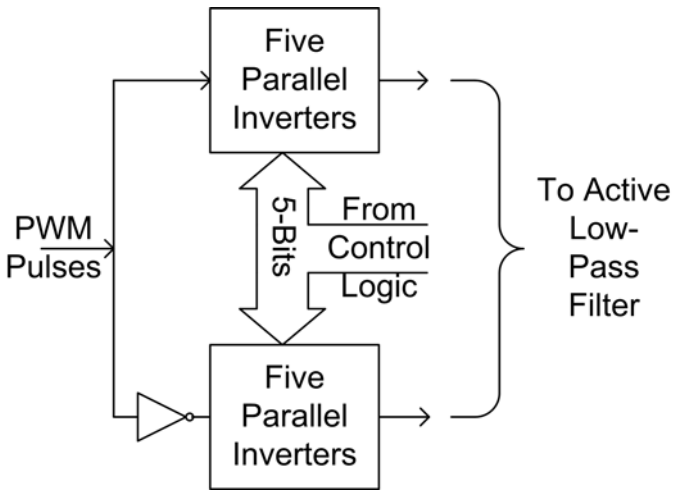


Figure 4.8: Architecture of the Class – D Output Stage and Coarse Control

As shown in Figure 4.8, one group of five inverters is used in each branch of the H-bridge to implement the class – D output stage and coarse control. The inputs to the block are the PWM pulses and 5-bit digital data from the control logic block. The output from the block is the coarsely controlled PWM pulses to the active low-pass filter. First, the PWM pulses are mutually inverted using an additional inverter in any one branch of the H-bridge.

The class – D output stage is usually implemented using inverters. The coarse control is designed using different current amplifiers. Hence, the class – D output stage and coarse control block is implemented using 5 parallel inverters with different current capacity. Different current capacity is achieved by using different width of the transistors used in inverters. Only one of the five parallel inverters is selected at any time. The gate inputs of all five inverters are connected to 5-bit input from the control logic block.

4.4.2 Implementation

The implementation of the class – D output stage and coarse control is shown in Figure 4.9.

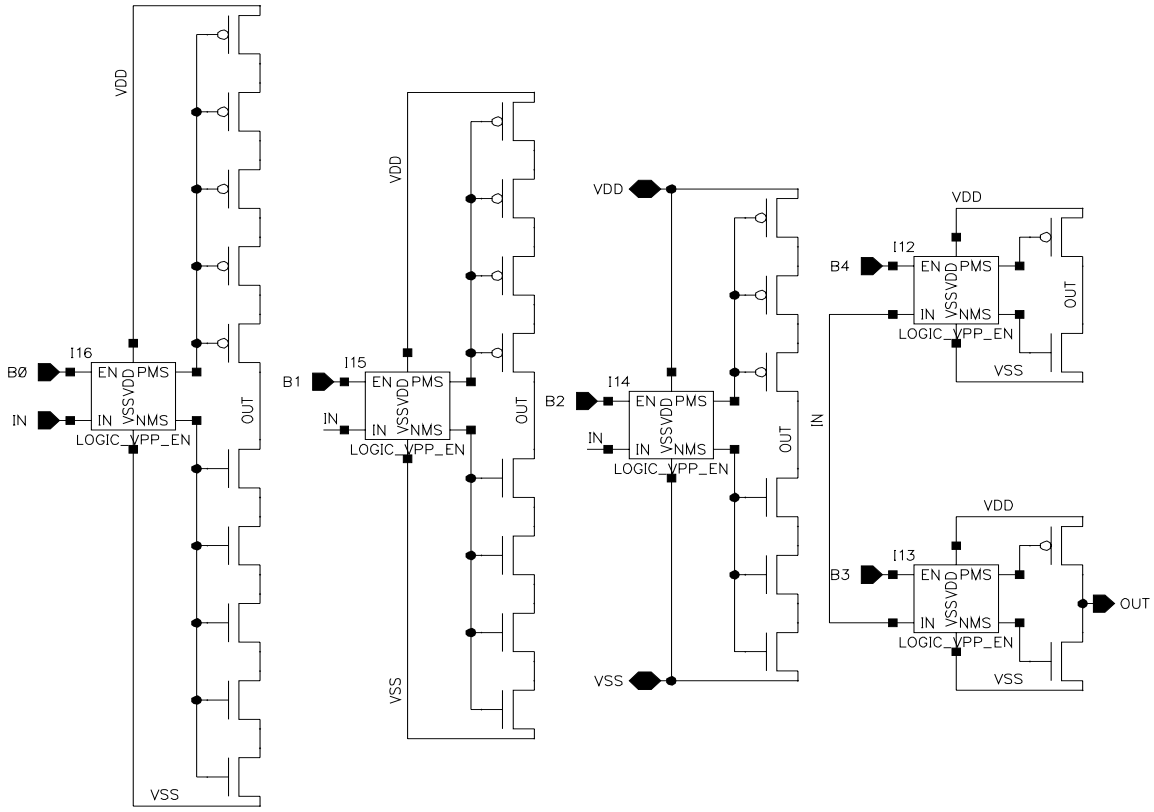


Figure 4.9: Implementation of the Class – D Output Stage and Coarse Control

As shown in Figure 4.9, the transistors with different widths are used in five parallel branches to implement coarse control with class – D output stage. The widths of NMOS and PMOS used in five parallel branches with respect to the output peak-to-peak voltage are shown in Table 4.1.

Required Peak-to-Peak Voltage (in V)	No. of transistors in series	Size of each transistor		Effective sizes of transistors	
		NMOS (in µm)	PMOS (in µm)	NMOS (in µm)	PMOS (in µm)
0.40	5	0.46	0.92	0.092	0.184
0.64	4	0.42	0.84	0.105	0.210
1.00	3	0.42	0.84	0.140	0.280
1.60	1	0.55	1.10	0.550	1.100
2.26	1	0.90	1.80	0.900	1.800

Table 4.1: Sizes of PMOS and NMOS in the Coarse Control Block with respect to Peak-to-Peak Voltage across Load Resistance

From Figure 4.9 and Table 4.1, the current flowing through the inverter decreases as number of transistors in series increases. Therefore, five inverters in series supply

lowest current and hence the lowest peak-to-peak voltage and power. On the other hand, only one PMOS and NMOS with larger width supplies highest current and peak-to-peak voltage.

The gate selection logic, shown in Figure 4.9, is designed such that when the enable input is at logic high level, the logic level at the input pin is passed to the gate of transistors. If enable input is at logic low level then gate to PMOS is pulled high and gate to NMOS is pulled low to turn off both type of transistors. The enable signal is supplied from the control logic.

The gate level implementation of the gate selection logic is shown in Figure 4.10.

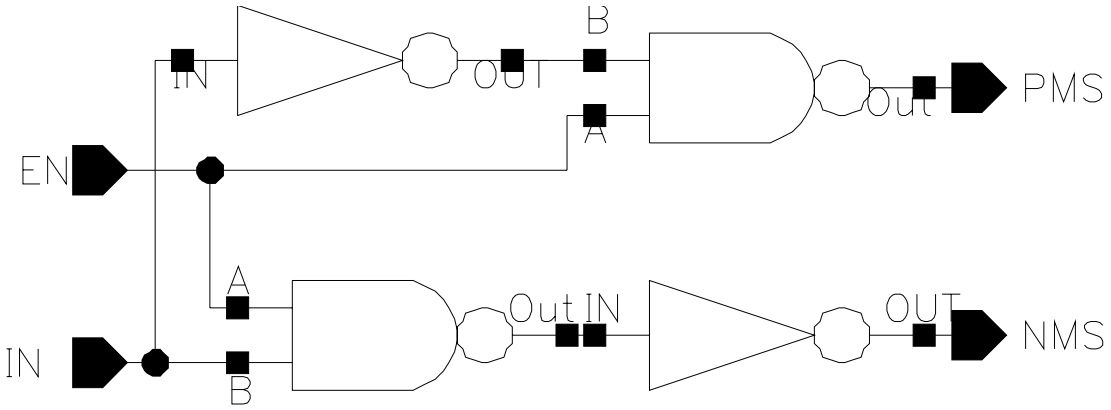


Figure 4.10: Implementation of the Gate Selection Logic

The gate selection logic has two inputs and two outputs and it is implemented using two NAND gates and two inverters. IN (input pulse) and EN (Enable) are the two inputs. PMS for the gate of PMOS and NMS for the gate of NMOS are the two outputs. When input EN is low, the outputs PMS is high and NMS is low. Hence, the PMOS and NMOS of the inverter are OFF. When EN is high, both outputs PMS and NMS receive the same logic level fed at input IN. Therefore, the gate selection logic is designed to work as a digital switch.

4.4.3 Simulation Results

The simulation waveforms obtained for the class – D output stage and coarse control for both H-bridge branches are shown in Figure 4.11.

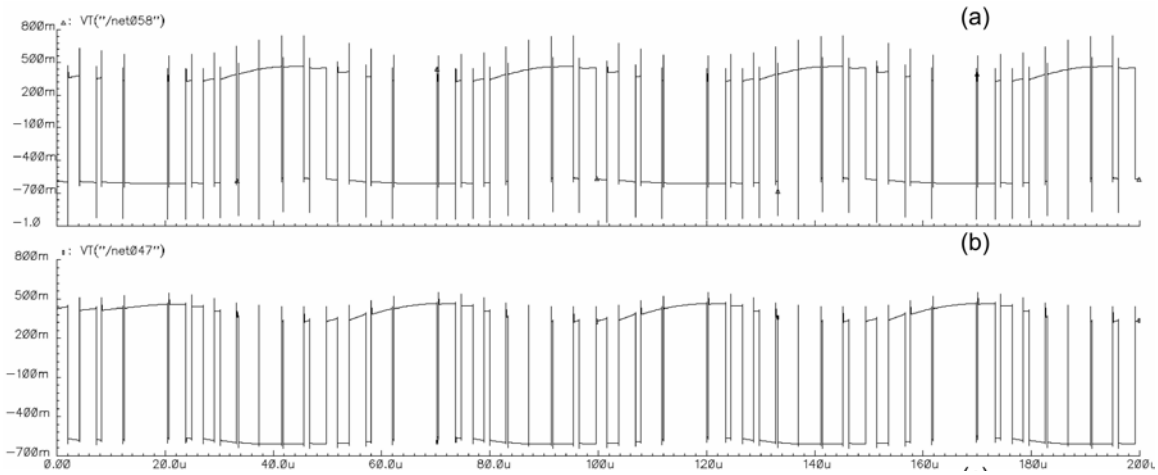


Figure 4.11: Simulation Waveforms for the Class – D Output Stage and Coarse Control in Both H-Bridge Branches

The simulation waveforms shown in Figure 4.11 are obtained for 2.26 V peak-to-peak output. The waveforms show the correct functioning of the block. The logic high level of both the waveforms is not flat because of the loading effect. And the glitches observed are also because of the loading effect.

The simulation results obtained by simulating different combinations of digital inputs are shown in Table 4.2.

Required Peak-to-Peak Voltage (in Volts)	Actual Peak-to-Peak Voltage (in Volts)	% Error
0.40	0.393	-1.75
0.64	0.630	-1.56
1.00	1.017	+1.70
1.60	1.600	0.00
2.26	2.216	-1.95

Table 4.2: Simulation Results obtained for Class – D Output Stage and Coarse Control

Table 4.2 shows us the desired values of peak-to-peak voltages, actual values of peak-to-peak voltage and the % error. The % error for worst case is less than ± 2%. Therefore, the desired coarse control functionality is achieved by the class – D output stage with coarse control block.

4.5 Active Low-Pass Filter

The active low-pass filter is designed to convert PWM pulses into sinusoidal sound waves. One active low-pass filter is used in each of the two branches of the H-bridge. Active low-pass filter is also used to block high frequency components to reduce the distortion of the output sound waves.

Second order, non-inverting, dual feedback configuration of the Butterworth filter [46] is chosen for the design of the active low-pass filter in the proposed design.

4.5.1 Architecture

The architecture of the active low-pass filter is shown in Figure 4.12.

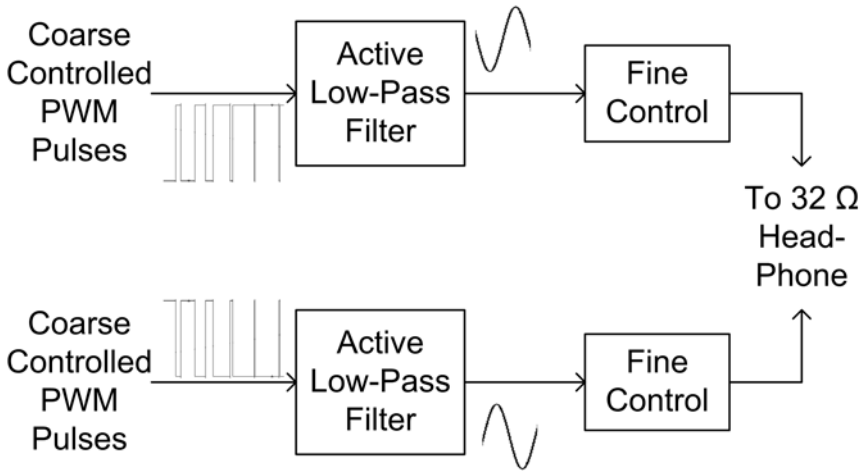


Figure 4.12: Architecture of the Active Low-Pass Filter

The active low-pass filter is used to convert the PWM pulses to sinusoidal sound waves. The filters can be classified as active filter and passive filter. In our design we used active filter. The sampling frequency is 244 KHz and the desired frequency response is from 20 Hz to 20 KHz. Hence, we designed active low pass filter.

From Figure 4.12, the input to the active low pass filter is controlled PWM pulses generated from the class – D output stage and coarse control block. The output is sinusoidal sound waves. The sinusoidal sound waves in both H-bridge branches have 180^0 phase difference.

4.5.2 Implementation

The active low-pass filter is implemented using two op-amps, resistors and

capacitors only. We used 2nd order, non-inverting, dual feedback configuration of the Butterworth Filter [46]. The implementation of the active low-pass filter of the proposed device for hearing-testing is shown in Figure 4.13.

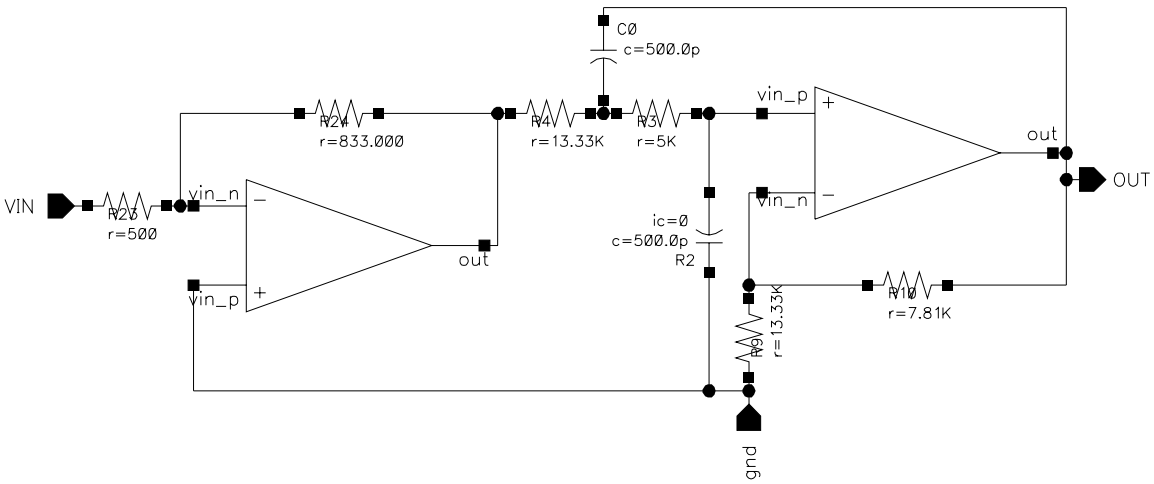


Figure 4.13: Implementation of the Active Low-Pass Filter

The active low-pass filter block is designed using two op-amps, six resistors and two capacitors. First op-amp is used in inverting amplifier configuration to adjust over-all gain of the filter. The gain of this inverting amplifier can be adjusted by selecting proper ratio of feedback resistor and input resistor. The second op-amp is used to implement 2nd order, non-inverting, dual feed-back configuration of the Butterworth filter [46]. The values of resistors and capacitors are calculated by considering 100 KHz cut-off frequency. The output stage of first amplifier is designed using normal size transistors but, the output stage of the filter op-amp is designed with large size transistors to supply sufficient current to the output.

The transistor level implementation of the op-amp is shown in Figure 4.14.

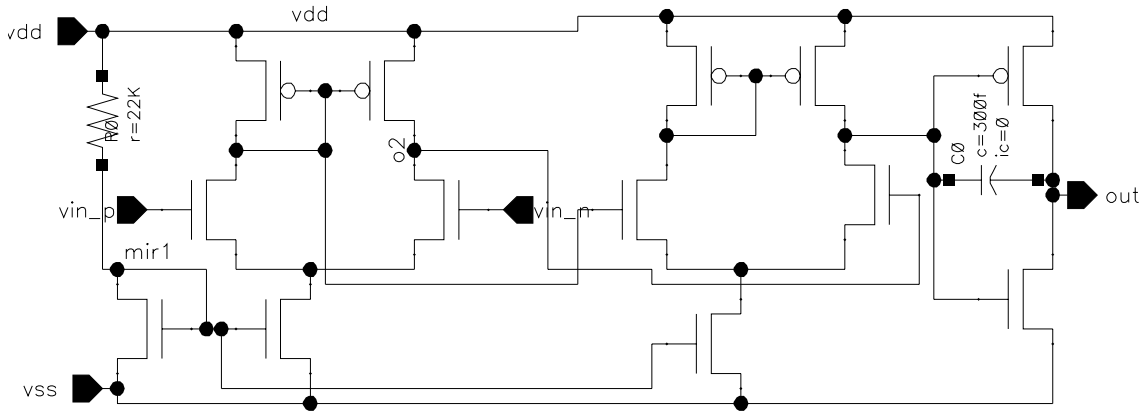


Figure 4.14: Implementation of the Op-Amp

As shown in Figure 4.14, the op-amp is designed using two stages of differential amplifier and one stage of output amplifier. The gain of the amplifier is decided by the gains of the two differential stages. The output amplifier stage is designed to achieve rail-to-rail output voltage swing. The main function of the output amplifier is to supply very high current at output and hence very low output resistance.

4.5.3 Simulation Results

The simulation waveforms for input and output of the active low-pass filter are shown in Figure 4.15.

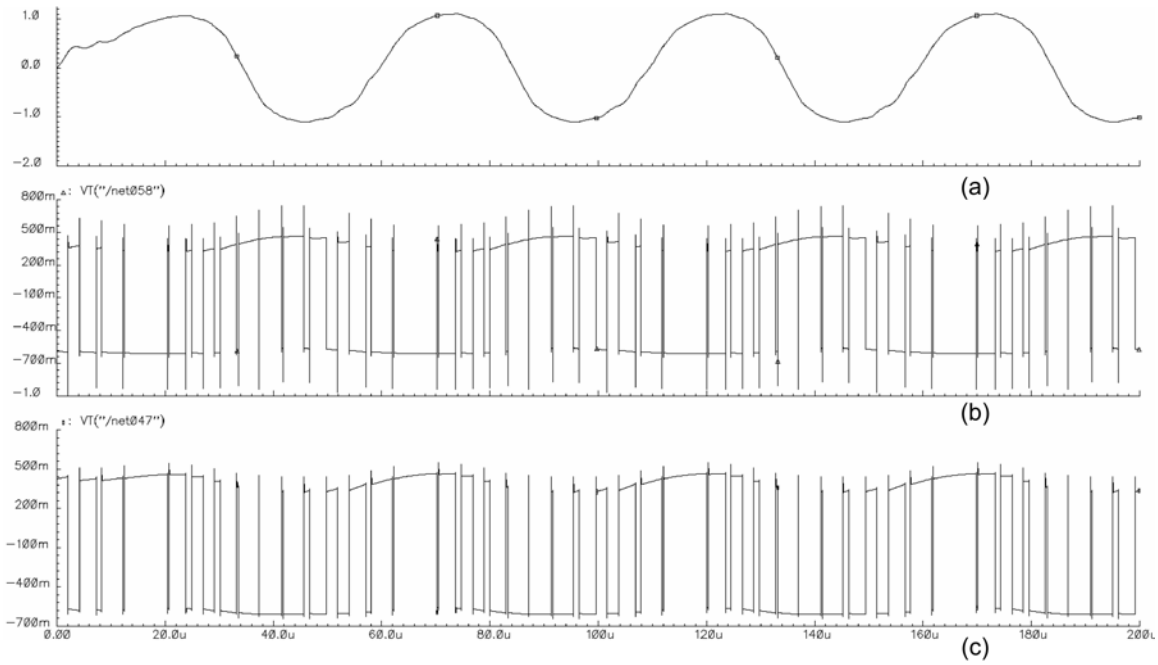


Figure 4.15: Simulation Waveforms for (a) Output of Active Low-Pass Filter (Across Head-Phones), (b) and (c) Input to Active Low-Pass Filter in Separate Branch of H-Bridge

Input PWM pulses, for 20 KHz digital input, are fed to both branches of H-bridge as shown in Figure 4.15(b) and (c). Figure 4.15(a) shows the output of the active low-pass filter across the 32 Ω load resistance. The 20 KHz output frequency with 2.26 V peak-to-peak voltage swing is shown. The measured distortion for 20 KHz sinusoidal wave is 10%.

Therefore, the functionality of the active low-pass filter is as desired.

4.6 Fine Control

This block is the second half of the whole control design. This is an important block for over-all control performance since accurate control steps are obtained by this control block. The purpose of previous control part (coarse control block) is to reduce peak-to-peak voltage applied to this fine control block. Reduction in peak-to-peak voltage to this block helps to reach minimum SPL level.

The fine control block is significant for all 16 sections of control to supply offset current and to provide steps of the fine control. It is intended to change (increase or

decrease) output SPL for every increment / decrement in the 7-bit control value. The functioning of the overall control can be understood easily using an example. For the control value of 90, 7-bit binary value (B0 – B6) of 90 is fed to the control logic block. The control logic block will configure the coarse control to supply 0.4 V peak-to-peak. From the Equation – 4.6, we can calculate the peak-to-peak voltage required for 90 dB SPL output is 0.16 V. Hence, the control logic will configure the fine control off-set network and fine control steps network to attenuate the 0.4 V generated by the coarse control block. After attenuation of the fine control block, 0.16 V peak-to-peak voltage is applied to the output. Similarly, for the control value equivalent to 100, the desired peak-to-peak voltage calculated from Equation – 4.6 is 0.505 V. For 100 control value, the coarse control is configured to supply 0.64 V peak-to-peak. This 0.64 V peak-to-peak value is attenuated to around 0.6 V using the fine control offset network. 0.6 V peak-to-peak is further attenuated using the fine control steps network to feed 0.505 V peak-to-peak across the output. This two examples are explained in the Table 4.3 below.

7-bit control Value	Desired Peak-to-Peak Value across Load	Peak-to-Peak Voltage After Coarse Control	Peak-to-Peak Voltage After Fine Control Offset Block	Peak-to-Peak Voltage After Fine Control Steps Block
90	0.16	0.4	0.3	0.16
100	0.505	0.64	0.54	0.505

Table 4.3: Explanation of Control using Examples

4.6.1 Architecture

The fine control has two main blocks; first is the control steps and second is the control offset. The architecture of the fine control block is shown in Figure 4.16.

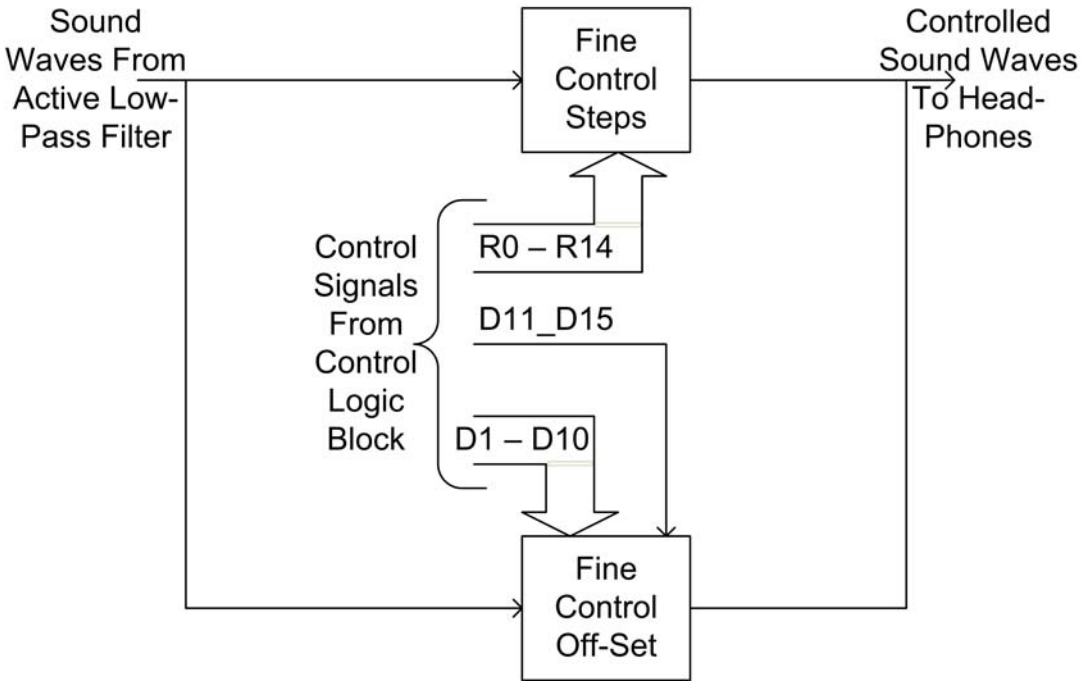


Figure 4.16: Architecture of the Fine Control Block

As shown in Figure 4.16, the fine control steps block and the fine control off-set block are connected in parallel to the input and output sound waves. The inputs to the block are coarsely controlled sinusoidal waves and 26 control signals (R0 to R14, D11_D15 and D1 to D10) from the control logic. The output from the block is finely controlled sound waves. Among the 26 inputs from the control logic, R0 to R14 (15 bits) are used to select a group of three TG network which is used for fine control steps. The rest of the decoder inputs, from D1 to D10 and D11_D15, are used to select any one of the 11 TG network of the fine control off-set.

The finely controlled steps are achieved by adding current flowing through the fine control steps and off-set. The current supplied by fine control off-set remains same for any particular section and changes with the change in section. On the other hand, current supplied from the fine control steps is changed for every unique input of 7-bit control register.

4.6.2 Implementation

The top level hierarchical blocks of the fine control block with the control logic is shown in Figure 4.17.

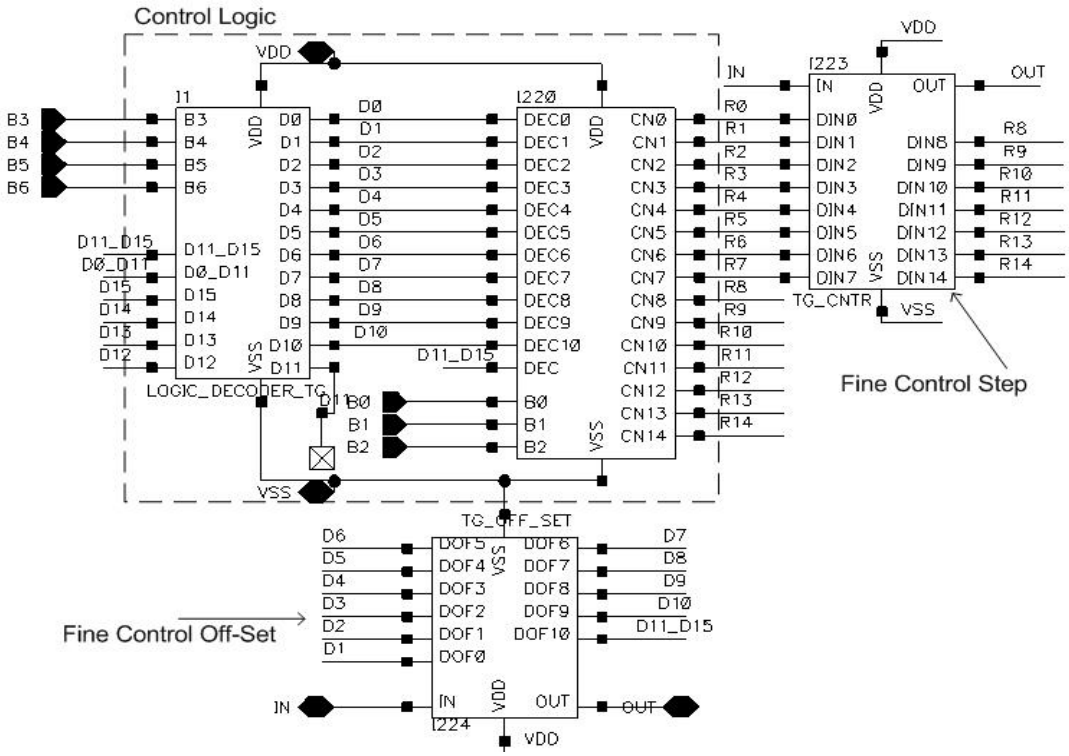


Figure 4.17: Implementation of the Fine Control Block with the Control Logic

The fine control step and off-set blocks are connected in parallel. The off-set block is controlled by decoder outputs (D1 – D10 and D11_D15) whereas steps block is controlled by the fine control step logic outputs (R0 – R14). Table 4.4 below shows selected group of three inputs for particular decoder output.

Enabled Decoder Output	Fine Control Step Inputs Selected
D0	R0, R1, R2
D1	R1, R2, R3
D2	R2, R3, R4
D3	R3, R4, R5
D4	R4, R5, R6
D5	R5, R6, R7
D6	R6, R7, R8
D7	R7, R8, R9
D8	R8, R9, R10
D9	R9, R10, R11
D10	R10, R11, R12
D11_D15	R12, R13, R14

Table 4.4: TG Array and Signal Selection According to D0 – D10 and D11_D15

In the pair of R_N, R_{N+1}, R_{N+2}, R_N supplies the lowest current and R_{N+2} supplies the highest current. Hence, R0 supplied the lowest and R14 supplies the highest current in the steps control block. The TG array connected with R0 – R14 inputs is shown in Table 4.5.

Input	Number of TG in Series	Width of NMOS and PMOS in each TG (in µm)	Effective Width of each TG (in µm)
R0	60	0.42	0.007
R1	30	0.42	0.014
R2	15	0.42	0.028
R3	8	0.42	0.0525
R4	4	0.42	0.105
R5	2	0.42	0.21
R6	1	0.42	0.42
R7	1	0.84	0.84
R8	1	1.68	1.68
R9	1	3.36	3.36
R10	1	6.30	6.30
R11	1	12.50	12.50
R12	1	25.00	25.00
R13	1	50.00	50.00
R14	1	100.00	100.00

Table 4.5: TG Array Connection with Each Input

As shown in Table 4.5, R_N TG array has double effective width than the previous (R_{N-1}) stage. For the TG network, the current is also doubled if the effective width is doubled. Hence, the control step and the slope of control are also doubled. The minimum step size is equivalent to 0.007 micron width and the maximum step size is equivalent to 25 micron width. Therefore, we can obtain large range of steps and slopes as required by the control design range.

4.6.3 Simulation Results

The plot of simulation results for 0 to 127 control value and dB SPL output across load of the fine control block is shown in Figure 4.18.

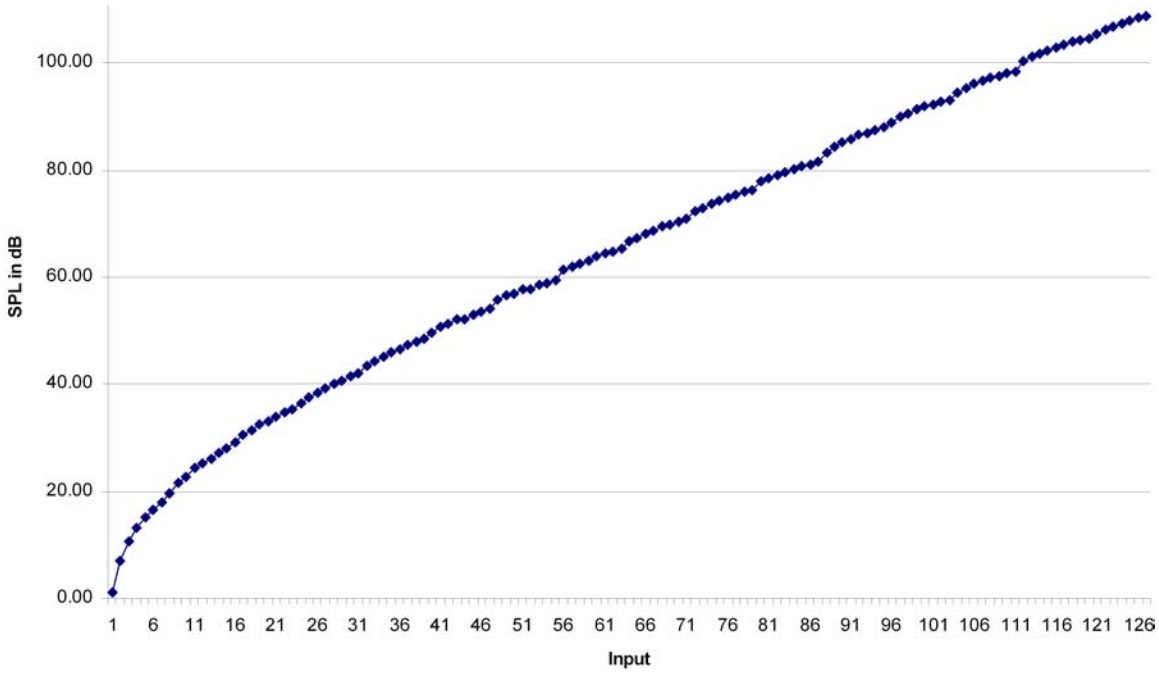


Figure 4.18: Plot of the Simulated Results Obtained for the Fine Control Block

As shown in Figure 4.18, the output sound waves are controlled from 1 to 109 dB SPL for digital control value from 0 to 127. A maximum step of 2 dB SPL is present for the output range from 15 to 109 dB SPL. Hence, the control is working satisfactorily without any glitches. The plot reflects desired functionality and control response. This control results are obtained for 20 KHz sound waves which is the worst case for any system. For lower frequency, they are more accurate and reliable.

The maximum output has reached 109 dB SPL only instead of desired 113 dB SPL because of the resistance of the TG switches. Even this output range is an acceptable achievement for the single-chip hearing-testing system.

4.7 Summary

First, we have explained the operation of the class – D output stage, control and filter section. Main design concerns for the active low-pass filter and other main blocks are also described. A detailed explanation of the control design is given.

The individual blocks of the class – D output stage, control and filter are described in detail. The detailed explanation of architecture is given for all the blocks.

The transistor level implementations are also described. Finally, authenticity and functionality of each block is proved using appropriate simulation waveforms and/or simulation results.

Chapter 5

Complete Design of the Single-Chip Device

5.1 Introduction

First, the importance and overview of the hearing-testing device will be described. Then, the complete design of the single-chip device for hearing-testing will be presented. The discussion and the implementation of the first of the two section of the complete design, the digital pulse-width modulator, will be provided. The validity and functional accuracy is proved based on the simulation results. The implementation and the simulation results of the second section, the class – D output stage along with the control and filter blocks will be discussed.

5.2 Main Design Concerns of the single-chip Device

In Chapter 3 and 4, all individual blocks of the single-chip device to be used in a hearing-testing system were discussed. The implementations and simulation results of each block are also provided.

In this chapter, the single-chip device, as a whole system, is tested through circuit simulations to prove its functionality after combining the two sections, covered in chapter 3 and 4, as shown in Figure 5.1.

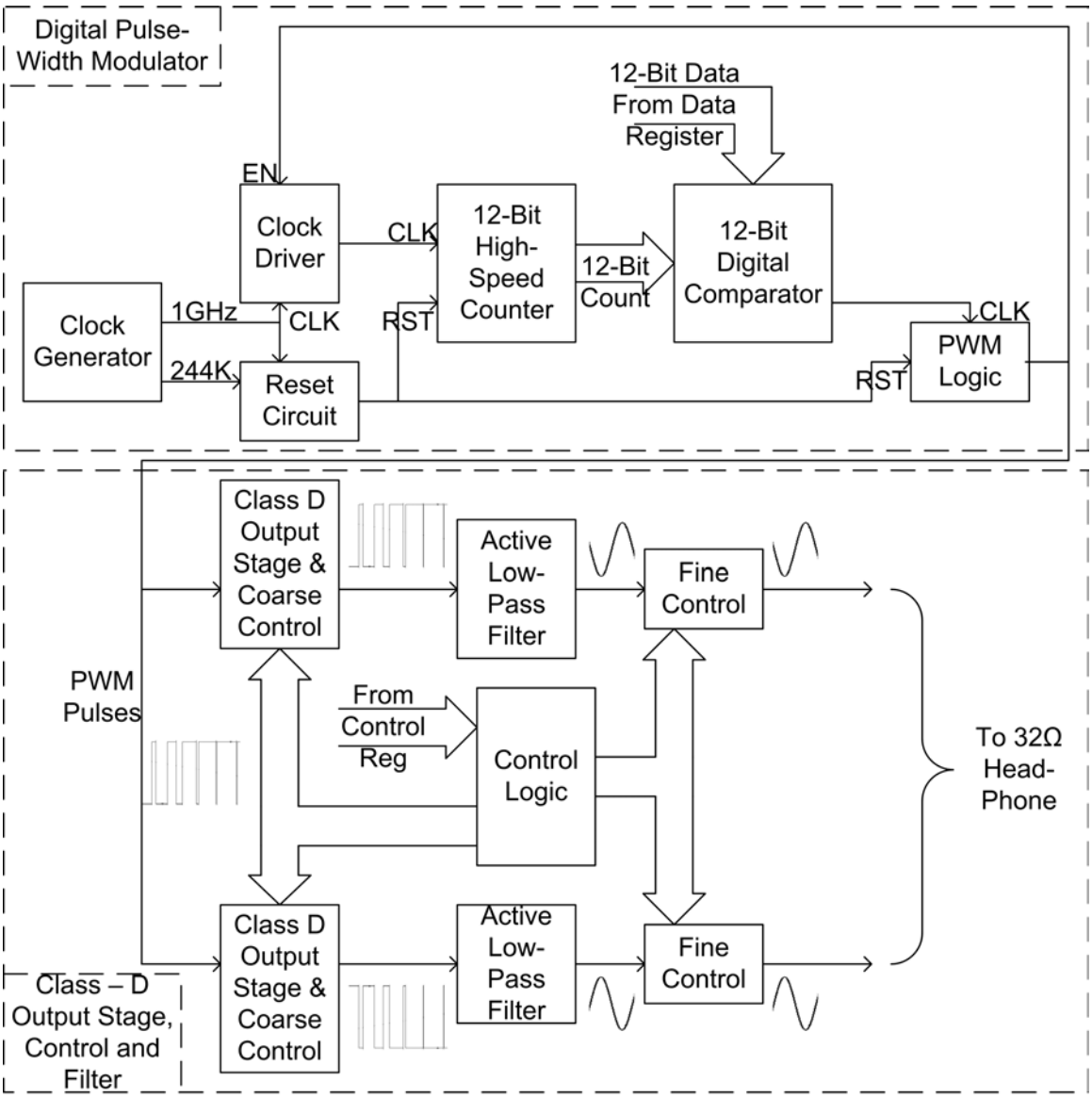


Figure 5.1: Architecture of the Device for hearing-testing

Some important design concerns, due to the implementation of the whole hearing testing device, are discussed next.

Loading is the first and foremost design consideration for integrating the hearing-testing system individual blocks. In CMOS based designs, capacitance is the main factor of loading. This load capacitance is mostly due to the input capacitance of the MOS transistors. Input capacitance increases with the width of the transistor. Higher capacitance takes longer time to charge and discharge causing longer propagation delay. Therefore, when all the individual blocks are combined together in a system, the input

capacitance can change the propagation delay and possibly the behaviour of the whole system. Though loading effect is already considered while designing individual blocks, the system should be tested for proper functionality and behaviour.

Simulation of the system requires long simulation time and very large data storage space. This limitation makes it more difficult to simulate the system at lower audio frequencies.

The full hearing-testing device is divide into two main sections namely, the digital pulse-width modulator and the class – D output stage, control and filter. Each section of the chip for hearing-testing is discussed in the following sections.

5.3 Digital Pulse-Width Modulator

The overview and explanation of architecture of the digital pulse-width modulator is already done in Chapter – 3. A brief explanation of this section is given below.

The digital pulse-width modulator section is designed to generated PWM pulses from 12-bit data register value which corresponds to the sinusoidal audio frequency. This section is designed using only digital design techniques. The implementation of the section is presented in the following sub-section.

5.3.1 Implementation

The implementation of the digital pulse-width modulator using individual internal blocks is shown in Figure 5.2.

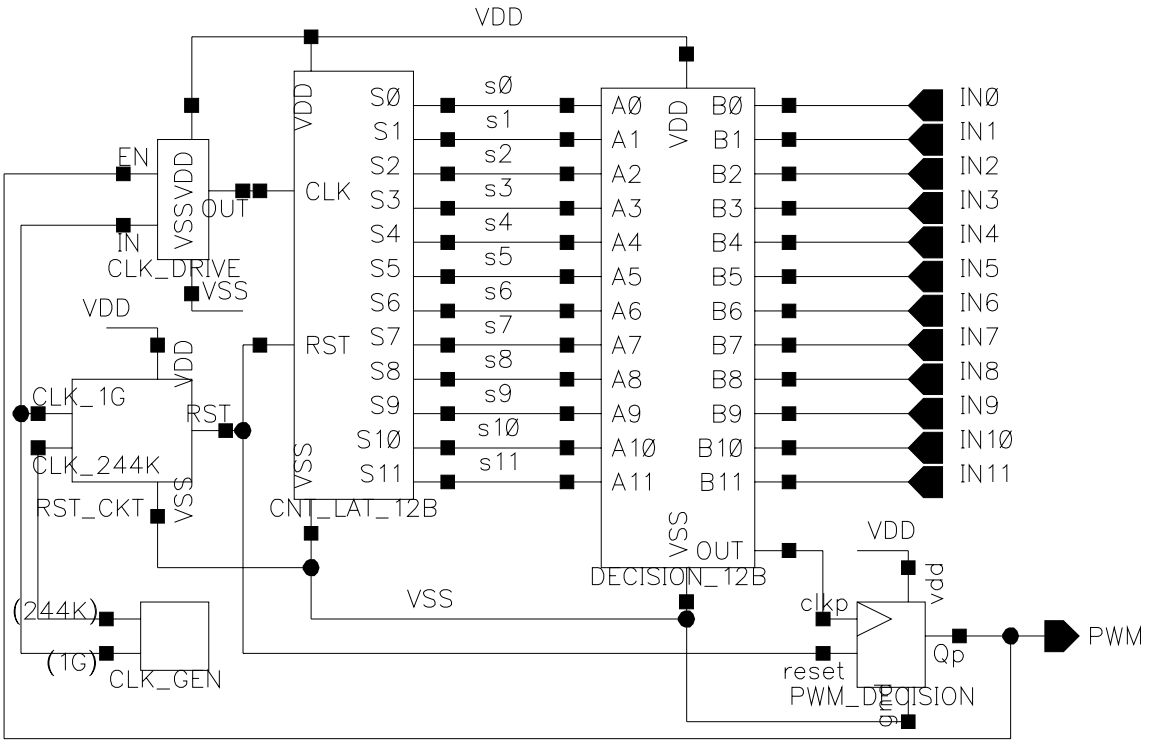


Figure 5.2: Implementation of the Digital Pulse-Width Modulator Section

As shown in Figure 5.2, the input to this section is the 12-bit digital data. This 12-bit digital data represents digital values of the sinusoidal audio waves. The output generated from the section is PWM pulses according to the 12-bit digital data.

The digital data source, for the 12-bit digital data, is designed using the pulse generator and transmission-gate based switches. The digital data source is designed to supply a 12-bit digital data for a 20 KHz sinusoidal wave. The 12-bit digital data will update at the rate of 244 KHz frequency. The 12-bit digital value for any frequency can be calculated from Equation 5.1:

$$Digital \quad Value(12-Bit) = 2048 \bullet (1+\sin(2 \bullet \pi \bullet f \bullet t)) \tag{5.1}$$

Where, f is the frequency of sinusoidal wave (sound wave) and

t is the time step.

Time step for our application will be 4.1499 μs since a sampling frequency of 244 KHz is used for the proposed hearing-testing device. Therefore, for 20 KHz frequency,

12-bit digital value at different time steps can be calculated by Equation 5.2,

$$Digital \quad Value(12-Bit) = 2048 \bullet (1 + \sin(40 \bullet \pi \bullet 10^3 \bullet t)) \tag{5.2}$$

One cycle of sinusoidal wave for 20 KHz can be generated by using 12 different time steps. For longer time simulation, we can use repetition of same cycle periodically.

Because of the storage space and simulation time limitation, all the blocks and the whole system is simulated at 20 KHz frequency which is the highest required frequency for the proposed device for hearing-testing. This 20 KHz frequency testing is the worst case for the proposed design. At this frequency, there will be maximum total harmonic distortion in the sound waves.

The simulation test-bench designed for the digital pulse-width modulator is shown in Figure 5.3.

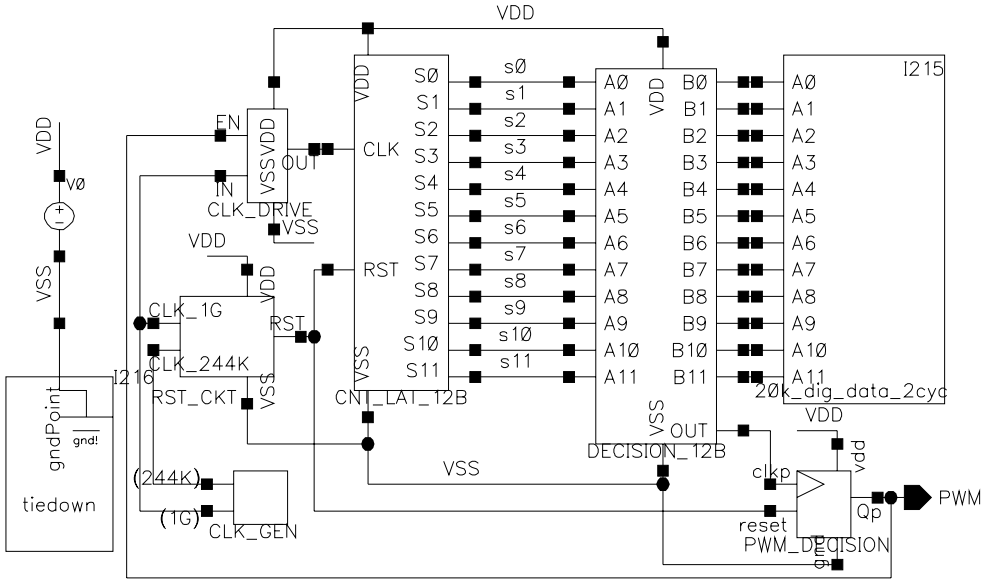


Figure 5.3: Simulation Test-Bench for the Digital Pulse-Width Modulator

As shown in Figure 5.3, the simulation test-bench for the digital pulse-width modulator can be generated by adding 1.3 V power supply and 12-bit digital input corresponding to a 20 KHz sinusoidal wave.

5.3.2 Simulation Results

By using the generated digital value as input to the digital pulse-width modulator section, the simulated output waveform, in the form of PWM pulses, are obtained and shown in Figure 5.4.

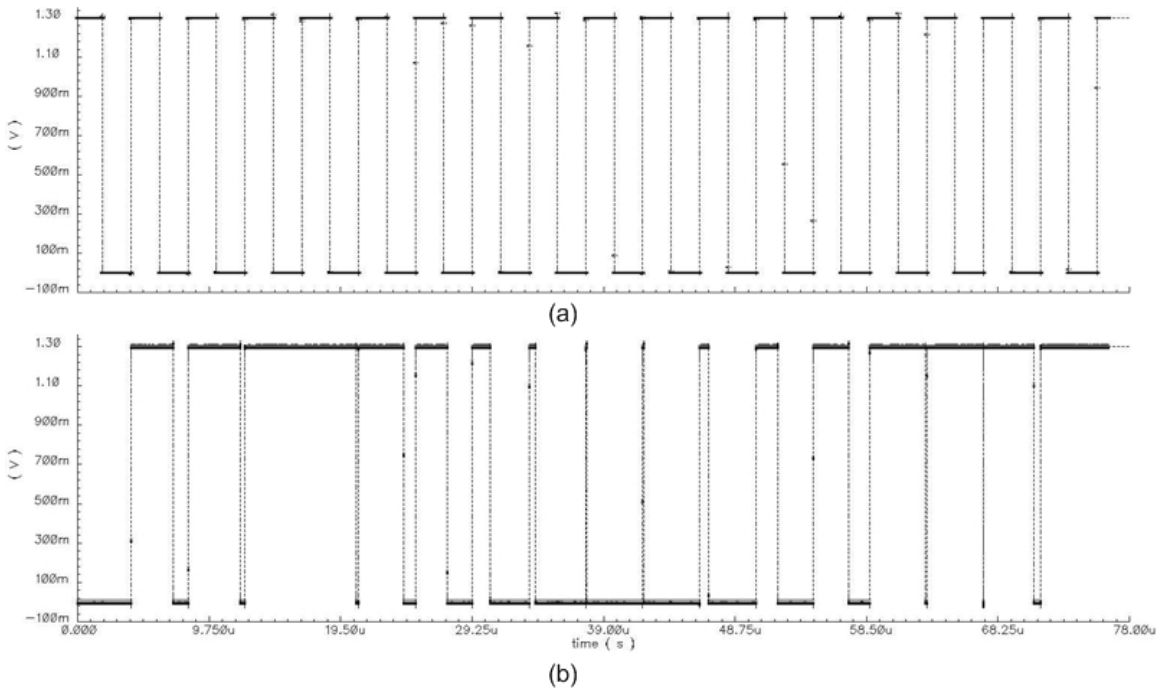


Figure 5.4: Simulation Waveforms : (a) 244 KHz Clock and (b) PWM Pulses for 20 KHz Sinusoidal Wave

As shown in Figure 5.4(b), the simulation waveform closely matches the simulation waveform of the PWM logic block shown in Figure 3.25(d) in Chapter 3. The capacitance loading didn't affect the functioning of the digital pulse-width modulator. The loading effect is not so significant because only two minimum size inverters are used at the input of the next section (class – D output stage, control and filter). The functional validity and accuracy of the digital pulse-width modulator section is demonstrated.

5.4 Class – D Output Stage, Control and Filter

The overview and the main design concerns of the class – D output stage, control

and filter section are already given in Chapter – 4. A brief description is mentioned here.

This section generates controlled sinusoidal sound waves from the PWM pulses fed from the digital pulse-width modulator section. The sound waves generated have mutual 180^0 phase difference to generate fully differential sound waves across the load resistor. The implementation and simulation results of this section are described in the following sub-sections.

5.4.1 Implementation

The implementation of the class – D output stage, control and filter section is shown in Figure 5.5.

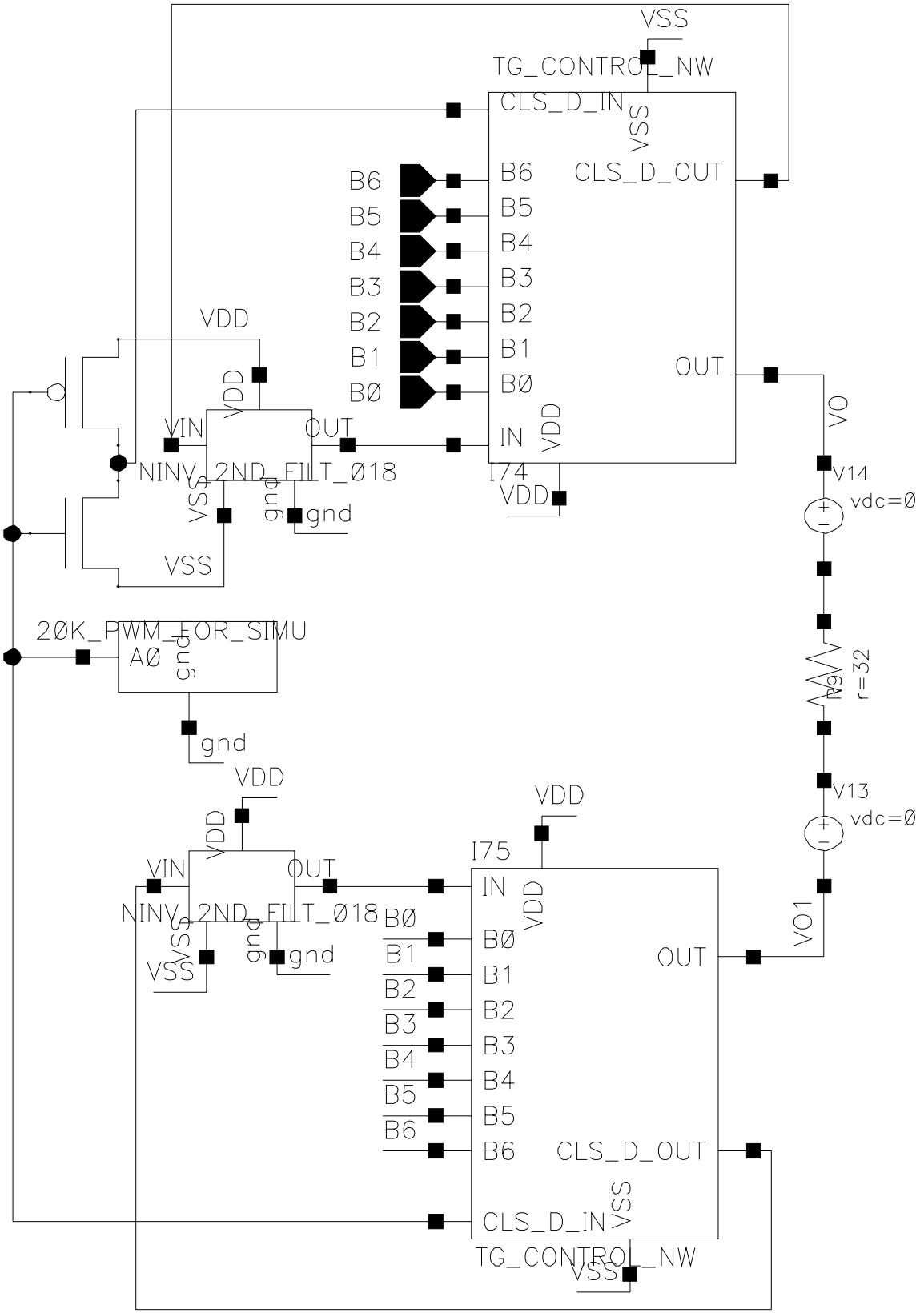


Figure 5.5: Implementation of the Class – D Output Stage, Control and Filter Section

As shown in Figure 5.5, the control logic, class – D output stage and coarse control and fine control are integrated in a single block. The inputs required for this section are the PWM pulses generated from the digital pulse-width modulator section and the 7-bit control value. The output generated is fully differential sinusoidal sound waves which are applied across a 32 Ω load resistance.

To obtain the simulation results for this section, the PWM pulses similar to the one generated in previous section (digital pulse-width modulator) should be generated. To generate similar PWM pulses, the time period for every cycle is measured using SpectreS simulation tool. The similar PWM pulses are generated using PWL (piece wise linear) voltage source. These PWM pulses correspond to 20 KHz sinusoidal frequency. Therefore, the output across the 32 Ω load should be a sinusoidal sound wave of 20 KHz frequency.

A 7-bit data for control input is also needed for simulation which is generated using seven pulse sources. These sources are configured such that the control value is increased by '1' after every complete cycle. The control value is changed from 0 to 127. The simulation result of the controlled output is obtained for all possible control values.

The simulation test-bench designed for the class – D output stage, control and filter section is shown in Figure 5.6.

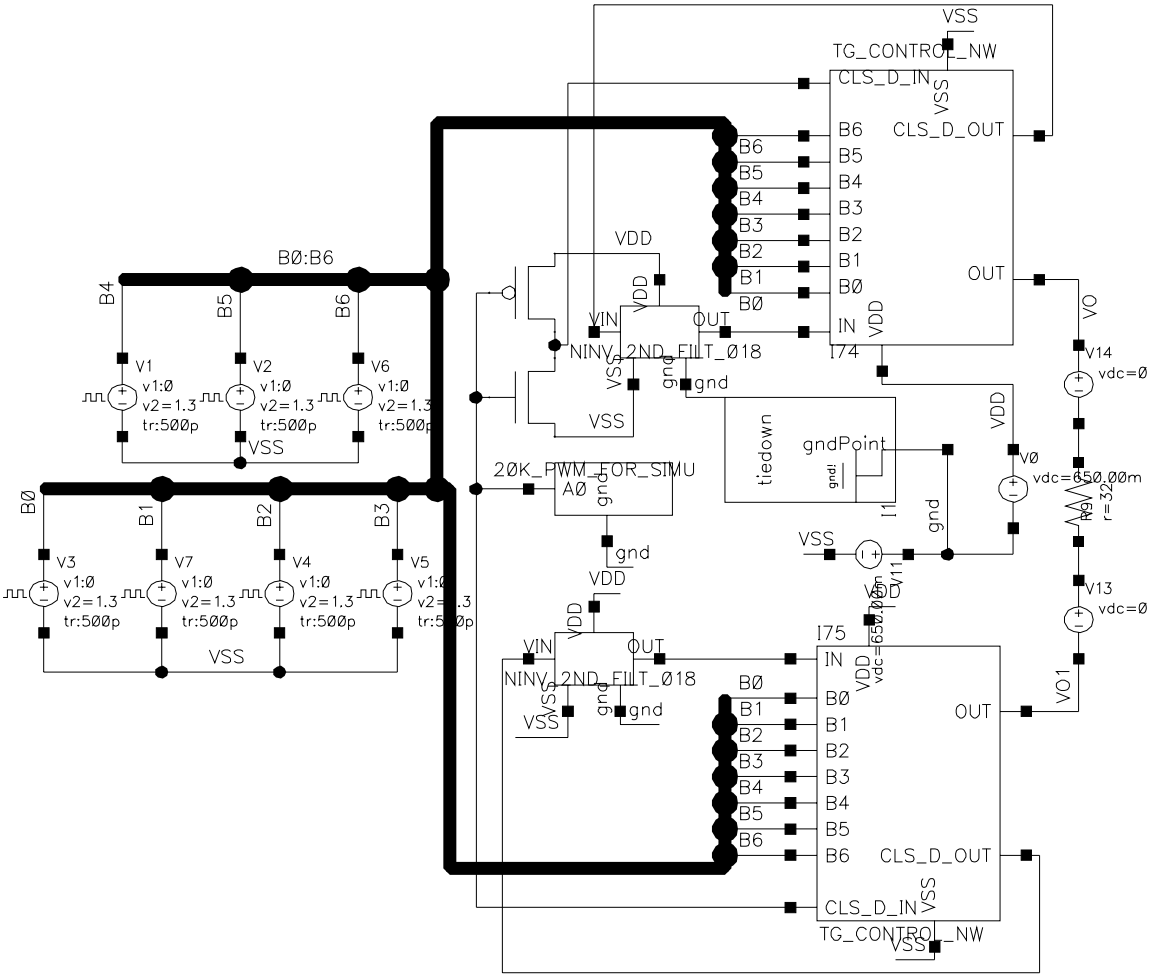


Figure 5.6: Simulation Test-Bench for the Class – D Output Stage, Control and Filter

As shown in Figure 5.6, the test-bench can be created by inserting the power supply and the 7-bit control value. The PWM pulses are fed from the designed block. A 32 Ω resistance is connected at the output to substitute head-phones. The voltage source of 0 V in series of 32 Ω is used to measure current flowing through the load resistance. The differential voltage across 32 Ω load resistance is also measured.

5.4.2 Simulation Results

The simulation waveform across the 32 Ω load resistance for "127" control value is shown in Figure 5.7.

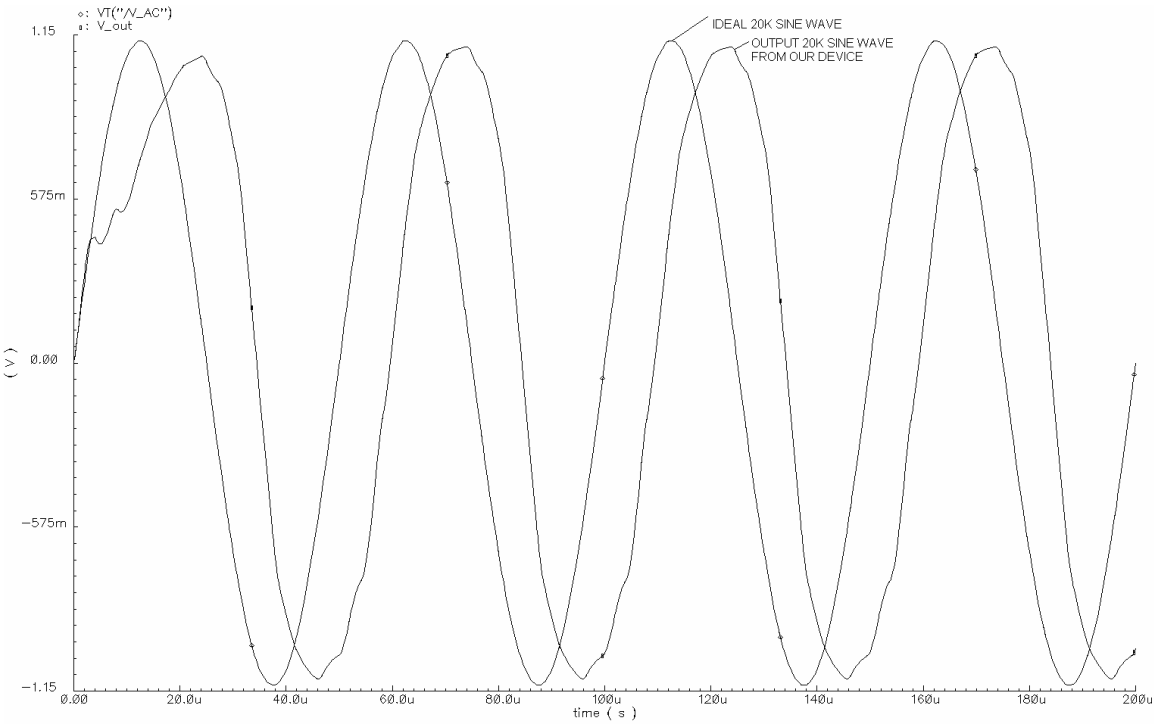


Figure 5.7: Simulation Waveform for Maximum Output

Figure 5.7 shows the simulation waveform of 20 KHz sound wave generated by this section. Ideal sinusoidal wave of 20 KHz is also plotted for the comparison of distortion and phase difference. As shown in Figure 5.7, total harmonic distortion for proposed design is 10%. The frequency of simulated waveform is also correct. The phase difference between the two waves is present because simulated wave depends on the PWM pulses fed to the system.

The simulation waveform of differential voltage across load resistance is shown in Figure 5.8. This waveform is simulated for control value from 0 to 127.

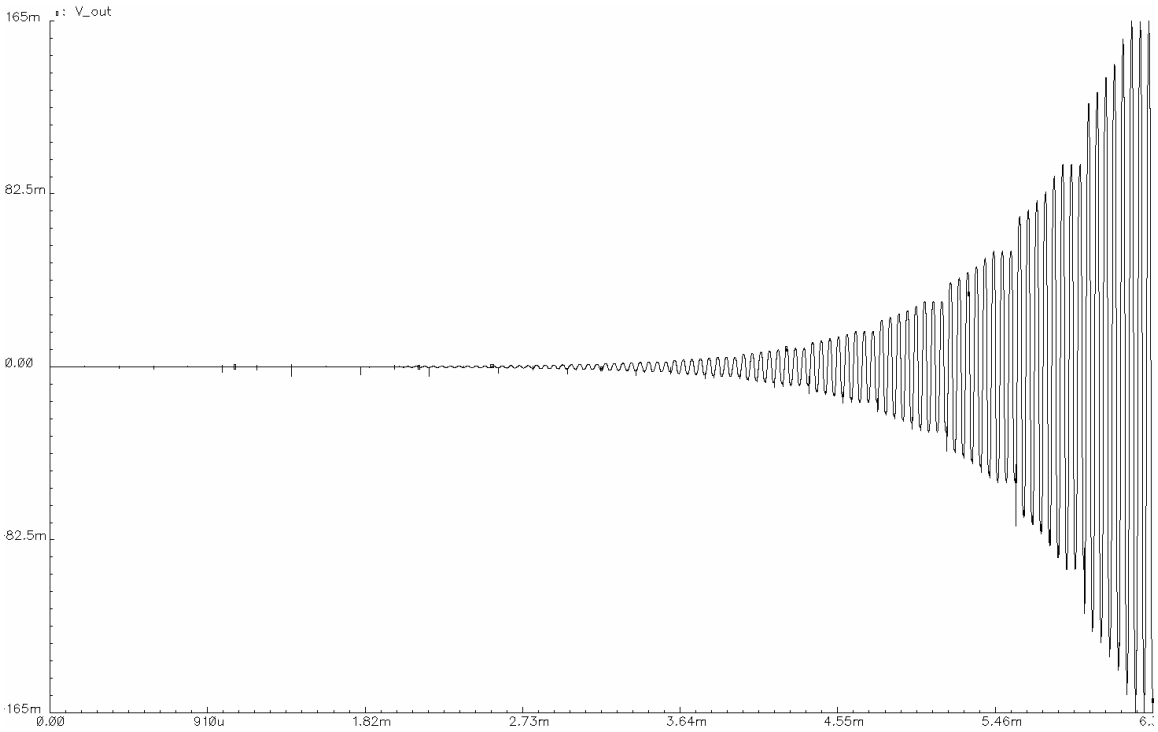


Figure 5.8: Peak to Peak Voltage Across Output For Digital Control Input

Figure 5.8 shows the simulation waveform of differential output across load resistance. The transient analysis for this waveform is swept for control value from 0 to 127. One cycle per control value is simulated. The peak of voltage output is changing exponentially similar to Figure 4.2. The output SPL equivalent to the peak-to-peak voltage obtained can be calculated using Equation 4.5.

The excel chart for the control value vs. output SPL is shown in Figure 5.9.

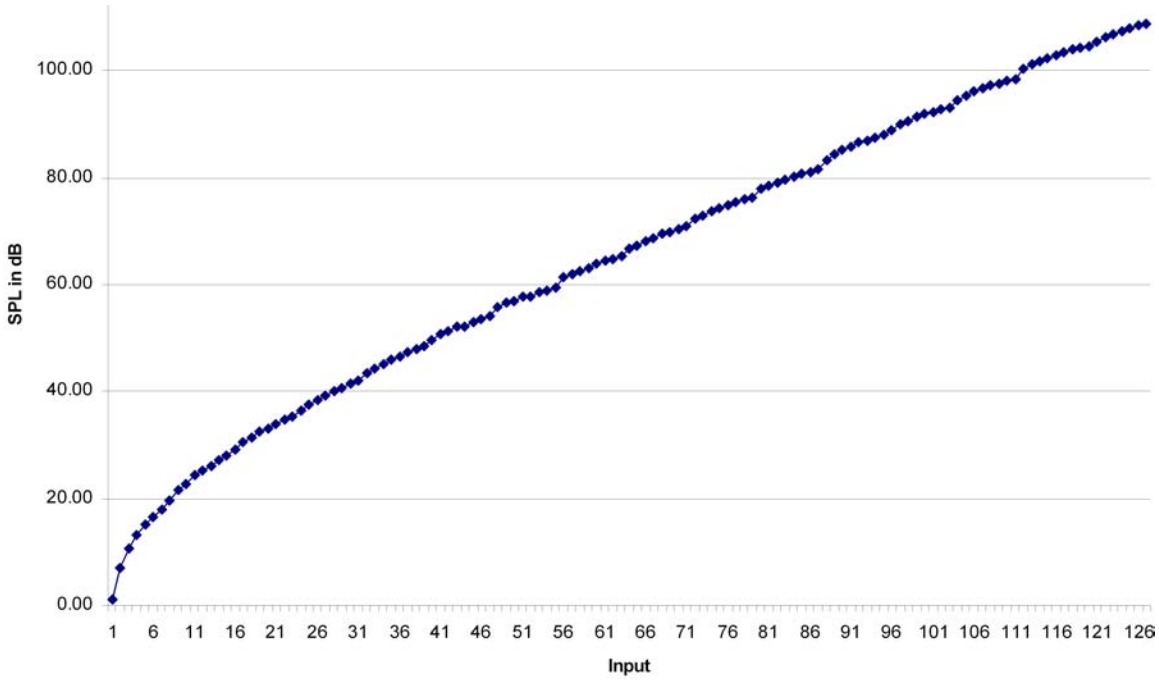


Figure 5.9: Excel Chart for SPL Output in dB for Control Inputs from 0 to 127

As shown in Figure 5.9, the output SPL is controlled from 1 to 109 dB SPL. A linear response is achieved for the range of 20 to 109 dB SPL. Maximum 2 dB SPL step is present from 15 to 109 dB SPL range.

From Figure 5.7, Figure 5.8 and Figure 5.9, the accuracy of the proposed device for hearing-testing is as desired. The desired functionality is also visible from these figures.

5.5 Summary

The overview and main design concerns of the proposed device for hearing-testing are explained. The system perspective of the proposed design is also discussed in detail. The two sections of the proposed device, namely the digital pulse-width modulator and the class – D output stage, control and filter are explained. The individual section implementation in CMOS 0.18 μm technology is described along with the simulation test-bench. The simulation results indicate the proper functionality of the designs.

Chapter 6

Conclusions

6.1 Introduction

This Chapter summarizes the contributions made in this thesis and the conclusions from the results obtained. It also discusses some important issues and the scope for further research in the area of the work presented.

6.2 Summary of Contributions

Chapter 2 reviews existing designs and recent trends of the different components of the hearing aids or device for hearing-testing. In this Chapter, we have introduced single chip design of hearing-testing system. Hence, throughout this thesis, we described different aspects of the device for hearing-testing.

In Chapter 3, we have presented design of the digital pulse-width modulator. This proposed design has notable improvements than the previous designs [24] - [30]. It consists of basic digital design blocks like clock generator, clock divider, clock driver, reset circuit, 12-bit high-speed counter, digital comparator and PWM logic block. The simulations are carried out to verify the authenticity and validity of this design. Some digital design blocks, like clock divider and high-speed counter, are designed to provide major improvements. We have improved the implementation of the clock divider by using D flip-flops (DFF) only compared to more complex designs [38] - [40] . A total of 12 DFF are used to generate a 244 KHz signal from a 1 GHz clock (divide-by-4096). The 12-bit high-speed counter is another block that has remarkable improvements over the previous designs [41], [42]. The lowest critical path delay in the previous designs for

12-bit or 16-bit was can be calculated using Equation – 3.2. Hence, the total critical path delay is 910.5 ps for the design of [42], when implemented in 0.18µm CMOS technology. For the proposed design, the critical path delay for 12-bit or 16-bit of counter remains the same, which is calculated using Equation – 3.4. The total critical path delay for the proposed design is only 389.75 ps. Hence, the proposed design offer 57.2 % lower critical path delay.

For the design in [42], 49 multiplexers are required. For static CMOS implementation, the total transistors needed for the design can be calculated as,49 x 14 = 686. Now, for the proposed design of the counter, total number of transistors required can be calculated using Equation – 3.5. The total transistors calculated are 288 transistors. Hence, we have saved 58 % transistors compared to the previous design. Area of the design is generally represented by the transistor widths (W). The transistor widths used by MUX, NAND, NOR, Sim. XOR and INV are 33W, 8W, 10W, 27W and 3W respectively. For the previous design of [42], the total transistor widths used is, 49 X 33 = 1617W. On the other hand, the total transistor widths occupied by the proposed design is calculated using Equation – 3.5 which is equal to 692W. Hence, the reduction in area by the proposed design is 57.2 %. Therefore, we can conclude that our design is faster and occupies less area then the previously proposed design [42]. This allowed the design of accurate 12-bit resolution in the proposed device for hearing-testing. The power consumption is also an important parameter for battery operated device. We have used special power reduction technique by implementing the clock driver. In our design, we have reduced switching by cutting off the clock signal to the 12-bit high-speed counter. This results in saving in power dissipation.

In Chapter 4, we have evaluated the second important section of the device for hearing-testing which is class – D output stage, control and filter. The biggest contribution in the proposed device is the control design which is central theme of this Chapter. Fully customized design of the control logic with high accuracy and reliable functionality is given. The coarse control is designed using digital design techniques only. The beauty of the coarse control design lies in its integration with class – D output stage. The control range from 1 to 109 dB SPL is achieved due to the use of the class – D output stage and coarse control block. Besides larger range of control, we have also

achieved accurate control steps ranging from 0.5 dB SPL to 2 dB SPL in the range of 15 to 109 dB SPL. These accurate control steps are achieved due to the fine control block. The fine control block is designed using the digitally programmable analog design. The transmission-gate based design is used to reduce the chip area. The low-pass filter is implemented using active devices to achieve very low on-chip area than its passive counterpart. The use of a 244 KHz sampling frequency and the 2^{nd} order of low-pass filter allowed a low harmonic distortion of the output sound waves.

In Chapter 5, we have addressed the device for hearing-testing as a system. The proposed device is designed on a single chip using 1.3 V power supply. The proposed design does not use any supply multipliers. Because of the larger control range and accurate resolution, the proposed device offers flexibility and controllability. An important aspect of the proposed device is that it does not use any analog-to-digital or digital-to-analog converter. The proposed design is designed for frequency response from 20 Hz to 20 KHz which is the largest response range in any hearing-testing or hearing aid devices. The output is also controlled from 1 to 109 dB SPL. Hence, the proposed device has the largest frequency response and the largest control range. Moreover, the proposed device for hearing-testing is designed using fully digital pulse-width modulator for accurate 12-bit resolution. Design techniques to reduce power and total harmonic distortion are also used.

6.3 Recommendations for Future Work

In the scope of the work presented in this thesis, there exists number of areas for further research and examination. They are explained in the following sub-sections.

6.3.1 Power Consumption

In this thesis, different techniques for power reduction are mentioned. Currently, the power dissipation for battery operated devices is a major concern. For longer battery life, power dissipation for any system should be as low as possible. Recently, development of different low-power design techniques is carried-out. The floating-gate based designs, multi-threshold designs, device operating in sub-threshold region are some

of the most popular ones. The possibility to integrate such techniques in the proposed device for hearing-testing should be considered as an important aspect. Novel research in the area of low power can be very helpful for the device for hearing-testing and the hearing aids.

6.3.2 Total Harmonic Distortion (THD)

Active low-pass filter with high sampling rate is used in the proposed design. Though the total harmonic distortion of the proposed device is within limit, it is important to reduce it further. Furthermore, the harmonic distortion for lower frequencies sound waves should be extracted from the appropriate simulations.

6.3.3 Improvement in Control Design

The over-all control of the proposed system is designed using analog and digital design techniques. The control offers a very large control range from 1 to 109 dB SPL for single-chip designs. In the fine control block, transmission-gates based active devices are used to achieve the desired level of current. The possibility of similar control characteristics using more efficient and lower area designs should be developed. Other designs like switched-capacitor based designs should also be checked for similar characteristics.

The control in the proposed design is implemented using curve fitting technique. More efficient and optimal solution for exponential control should be derived.

6.3.4 Design of USB Interface

This device for hearing-testing is PC programmable. The PC programmability is achieved by USB connection to the PC. The interface between input registers (12-bit data register and 7-bit control register) and PC should be designed for full functional system-on-a-chip.

Appendix A

Transistor Level Implementation of Logic Gates

In this appendix, we will describe transistor level implementation of all the logic gates and basic digital design blocks used in this thesis.

A.1 Inverter

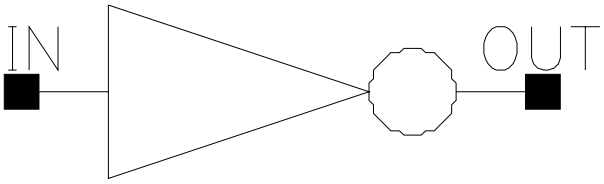


Figure A.1: Symbol of Inverter

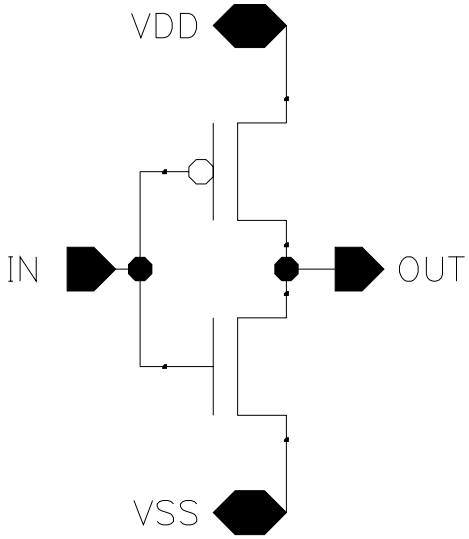


Figure A.2: Implementation of Inverter

A.2 NAND Gate

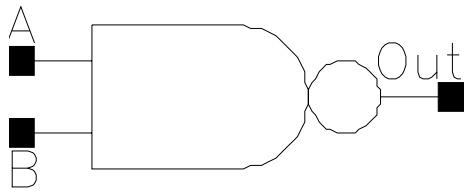


Figure A.3: Symbol of NAND Gate

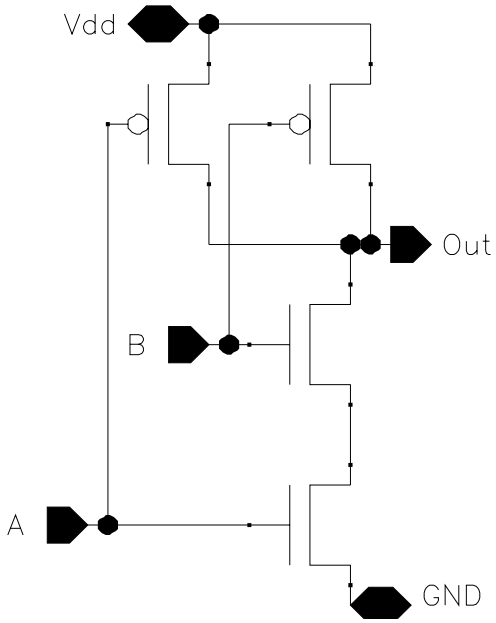


Figure A.4: Implementation of NAND Gate

A.3 3-Input NAND Gate

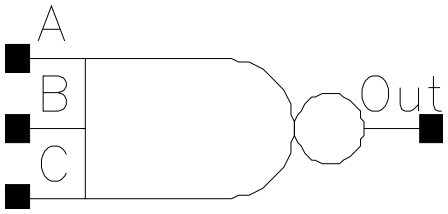


Figure A.5: Symbol of 3-Input NAND Gate

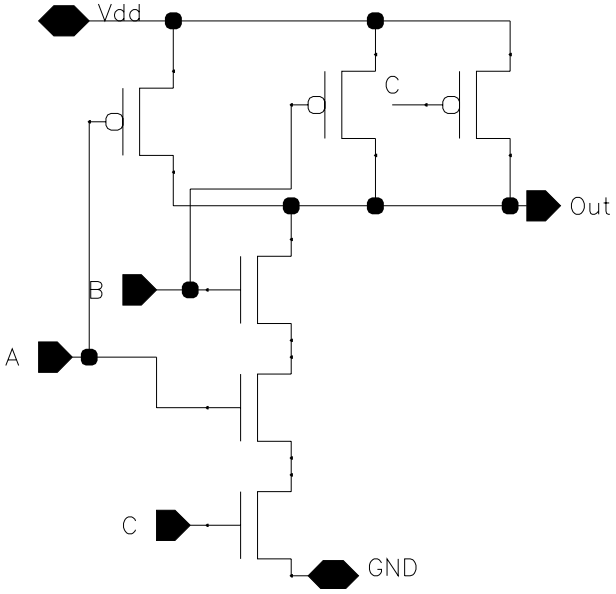


Figure A.6: Implementation of 3-Input NAND Gate

A.4 AND Gate

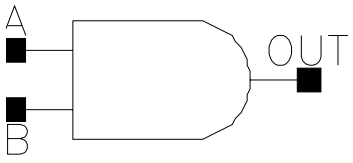


Figure A.7: Symbol of AND Gate

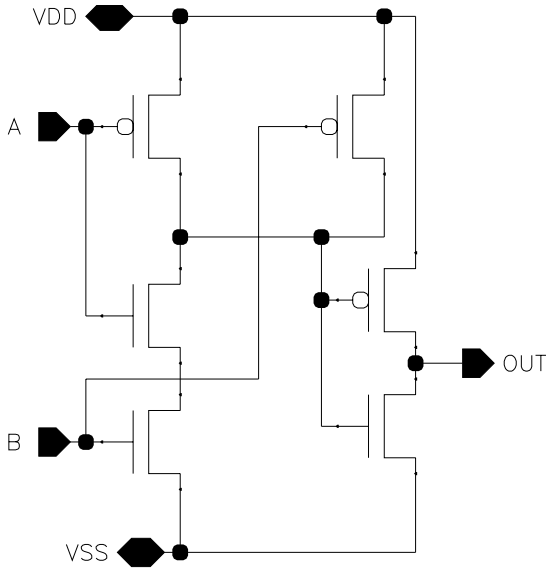


Figure A.8: Implementation of AND Gate

A.5 NOR Gate

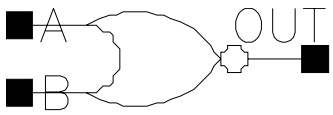


Figure A.9: Symbol of NOR Gate

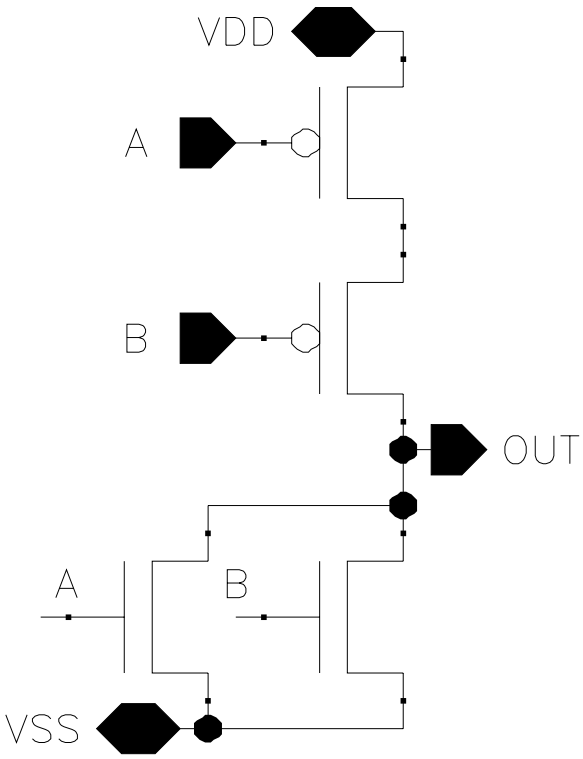


Figure A.10: Implementation of NOR Gate

A.6 XOR Gate

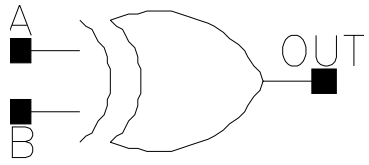


Figure A.11: Symbol of XOR Gate

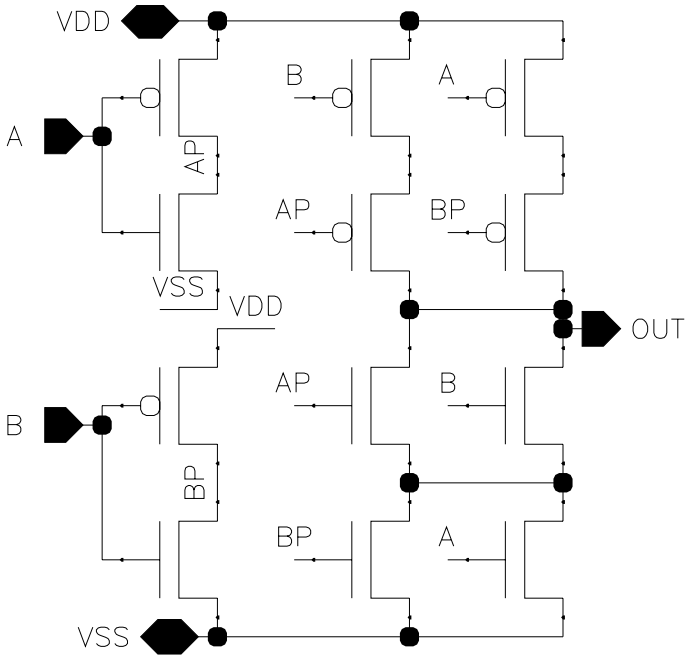


Figure A.12: Implementation of XOR Gate

A.7 Simplified XOR Gate

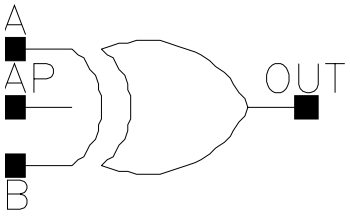


Figure A.13: Symbol of Simplified XOR Gate

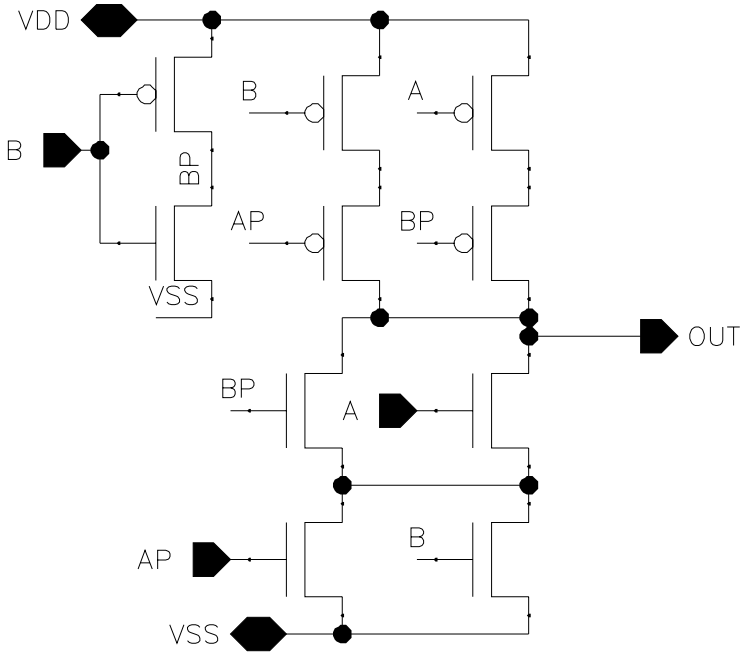


Figure A.14: Implementation of Simplified XOR Gate

A.8 XNOR Gate

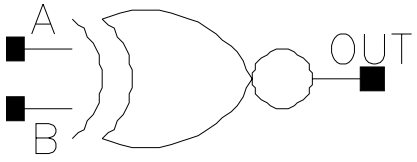


Figure A.15: Symbol of XNOR Gate

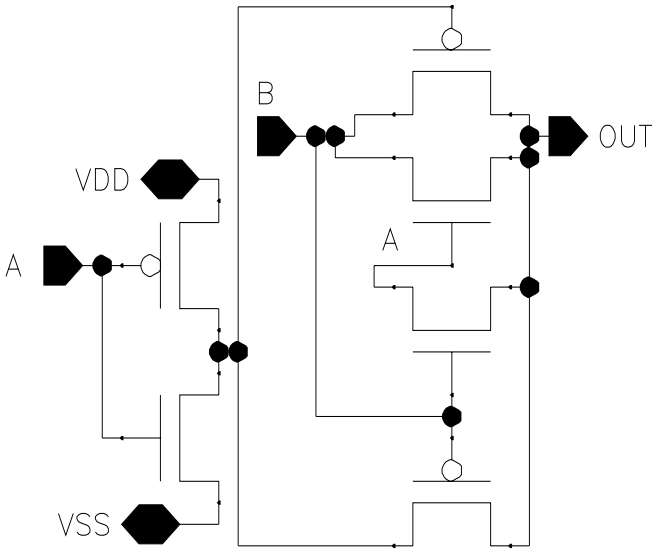


Figure A.16: Implementation of XNOR Gate

A.9 2-to-1 Multiplexer

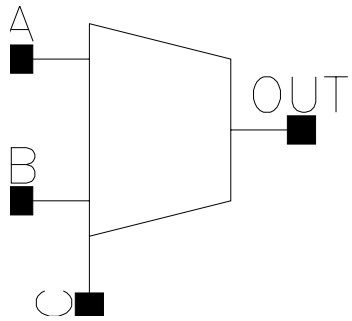


Figure A.17: Symbol of 2-to-1 Multiplexer

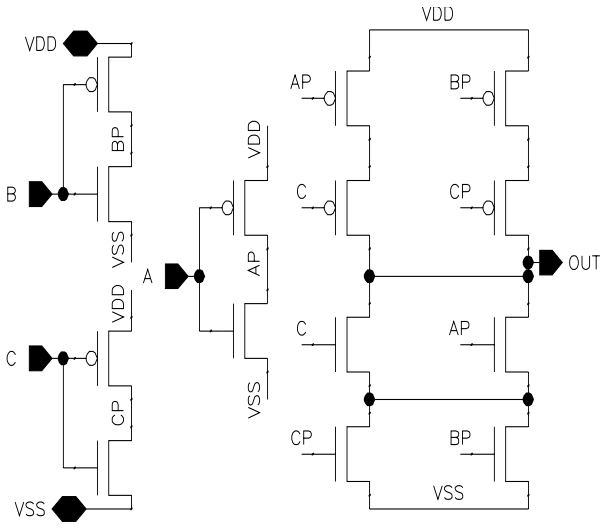


Figure A.18: Implementation of 2-to-1 Multiplexer

A.10 D Flip-Flop

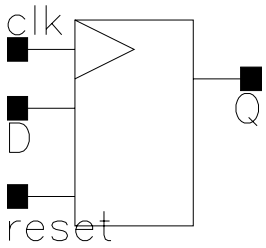


Figure A.19: Symbol of D Flip-Flop

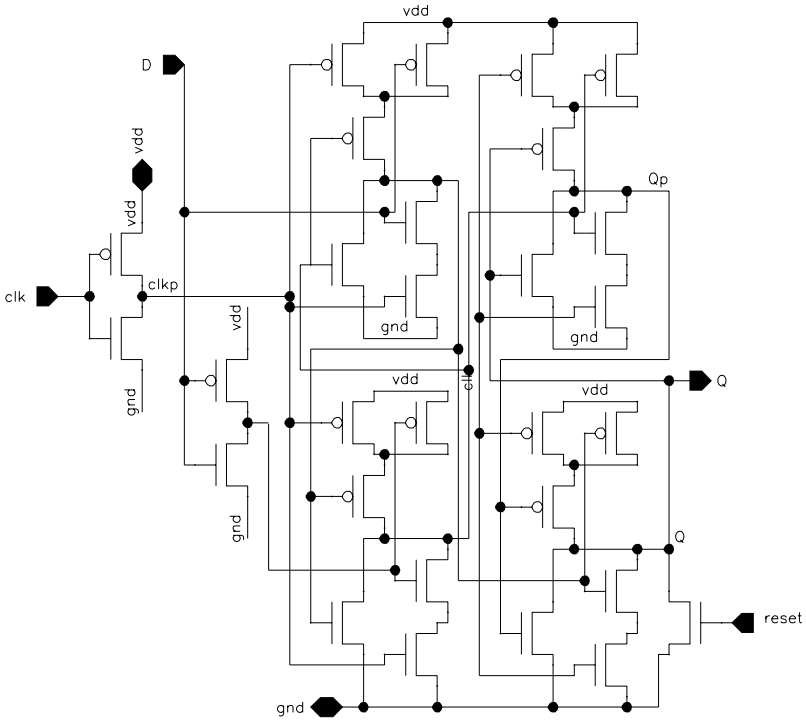


Figure A.20: Implementation of D Flip-Flop

Bibliography

[1] K. A. Mullins, "Design of a Digital Hearing Aid", *Northcon/96*, Seattle, WA, 4-6 Nov. 1996, pp. 281 – 284.

[2] A. M. Engebretson, "Benefits of Digital Hearing Aids", *IEEE Engineering in Medicine and Biology*, vol. 13, issue 2, April - May 1994, pp. 238 - 248.

[3] American National Standards Institute: *Specification of hearing aid characteristics*. In ANSI 3.22, ANSI, New York, 1987.

[4] IEC Technical Committee No. 29: *Electroacaustics, Hearing aids, part 0: measurement of electroacaustic characteristics*, In: IEC Standard 118-0, 2nd ed., Internation Electrotechnical Commission, 1983.

[5] IEC Technical Committee No. 29: *Electroacaustics, Hearing aids, part 2: measurement of electroacaustic characteristics*, In: IEC Standard 118-0, 2nd ed., Internation Electrotechnical Commission, 1983.

[6] A. C. van der Woerd, "Analog Circuits for a Single-Chip Infrared Controlled Hearing Aid," *Journal of Analog Integrated Circuits Signal Processing*, vol. 3, pp. 91 – 1.3, 1993.

[7] Francois Callias, Francois H. Salchli and Dominique Girard, "A Set of Four IC's in CMOS Technology for a Programmable Hearing Aid", *IEEE Journal of Solid State Circuits*, vol. 24, no. 2, April 1989.

[8] A. B. Bhattacharyya, R. S. Rana, S. K. Guha, R. Bahl and Sneh Anand, "A Micro-power Analog Hearing Aid on Low Voltage CMOS Digital Process", *9th International conference on VLSI Design*, Jan. 1996.

[9] D. Wayne, M. Rives, T. Huynh, D. Preves, and J. Newton, "A Single-Chip Hearing Aid with One Volt Switched-Capacitor Filters", *in Proceedings of IEEE Custom Integrated Circuits Conference*, 1992, pp. 7.5.1 – 7.5.4.

[10] G. Torelli, E. Chioffi and F. Maloberti, "A CMOS Micropower Input Amplifier for Hearing Aids", *Microelectron. Journal*, vol. 27, pp. 477 – 484, 1996.

[11] J. F. Duque-Carrillo, P. Malcovati, F. Maloberti, R. Perez-Aloe, A. H. Reyes, E. Sanchez-Sinencio, G. Torelli, and J. M. Valverde, "VERDI: An Acoustically

Programmable and Adjustable CMOS Mixed-mode Signal Processor for Hearing Aids Applications", *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 634 – 645, May 1996.

[12] J. Silva-Martinez, S. Solis-Bustos, J. Salcedo-Suner, R. Rojas-Hernandez and M. Schellenberg, "A CMOS Hearing Aid Device", *Journal of Analog Integrated Circuits and Signal Processing*, vol. 21, pp. 163 – 172, 1999.

[13] L. Pylarinos, N. W. Wong and K. Phang, "A Low-Voltage CMOS Filter for Hearing Aids Using Dynamic Gate Biasing", *in Proceeding of Canadian Conference on Electrical and Computer Engineering*, vol. 1, 2001, pp. 183 – 188.

[14] A. H. Reyes, E. Sanchez-Sinencio and J. Duque-Carrillo, "A Wireless Volume Control Receiver for Hearing Aids", *IEEE Transaction on Circuits and Systems II*, vol. 20, pp. 16 – 23, Jan. 1995.

[15] J. Silva-Martinez and J. Salcedo-Suner, "A CMOS Automatic Gain Control for Hearing Aid Devices", *in Proceedings on International Symposium on Circuits and Systems*, vol. I, 1998, pp. 297 – 300.

[16] H. Neuteboom, M. A. E. Janssens, J. R. G. M. Leenen, B. M. J. Kup, E. C. Dijkmans, B. de Koning, V. A. J. Frowijn, R. D. N. De Bleecker, E. J. van der Zwan, S. M. M. Note, Z. Wu, and S. R. Masschelein, "A Single-Battery, 0.9 V-Operated Digital Sound Processing IC Including AD / DA and IR Receiver with 2 mW Power Consumption", *in IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 1997, pp. 98 – 99.

[17] R. Klootsema, O. Nys, E. Vandel, D. Aebischer, P. Vaucher, O. Hautier, P. Bratschi and F. Bauduin, "Battery Supplied Low Power Analog-Digital Front-End for Audio Applications", *in Proceedings of European Solid-State Circuits Conference*, 2000.

[18] D. G. Gata, W. Sjursen, J. R. Hochschild, J. W. Fattaruso, L. Fang, G. R. Iannelli, Z. Jiang, C. M. Branch, J. A. Holmes, M. L. Skorcz, E. M. Petilli, S. Chen, G. Wakeman, D. A. Preves and W. A. Severin, "A 1.1-V 270 μA Mixed-Signal Hearing Aid Chip", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1670 – 1678, Dec. 2002.

[19] P. Favrat, P. Deval and M. J. Declercq, "An Improved Voltage Doubler in A Standard CMOS Technology", *in Proceedings of IEEE Internation Symposium on Circuits and Systems*, vol. 1, 1997, pp. 249 – 252.

[20] E. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips", *IEEE Journal of Solid-State Circuits*, vol. Sc-12, no. 3, pp. 657 – 665, June 1985.

[21] H. Levitt, "Digital Hearing Aids: A Tutorial Review", *Journal of Rehabilitation Research and Development*, vol. 24, pp. 7-20, Fall 1987.

[22] A. M. Engebretson, R. E. Morley and G. R. Popelka, "Development of an Ear-Level Digital Hearing Aid and Computer-Assisted Fitting Procedure: An interim report", *Journal of Rehabilitation Research and Development*, vol. 24, pp. 55 – 64, Fall 1987.

[23] L. Shao and B. E. Pfingst, "An Integrated Real-Time Computerized Hearing Testing System", *Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 1989. Images of the Twenty-First Century*. 9-12 Nov. 1989 Page(s):1967 - 1968 vol.6.

[24] J. Varona, A. A. Hamoui and K. Martin, "A Low-Voltage Fully-Monolithic Delta-Sigma Based Class-D Audio Amplifier", ESSCIRC – 2004, *29th European Solid-State Circuits Conference*, 2003, pp. 545 – 548.

[25] I. Y. Taha, M. Ahmadi and W. C. Miller, "A Sigma-Delta Modulator for Digital Hearing Instruments Using 0.18 μm CMOS Technology", *Proceedings of the 4th IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC '04)*, 19 – 21 July 2004, pp. 233 – 236.

[26] W. Marshall Leach, Jr., *Introduction to Electroacoustics and Audio Amplifier Design*, Second Edition – Revised Printing, Published by Kendall/Hunt, 2001.

[27] Jun-woo Lee, jae-shin Lee, Gun-sang Lee and Suki Kim, "A 2W BTL Single Chip Class-D Power Amplifier with Very High Efficiency for Audio Applications", ISCAS – 2000, *IEEE International Symposium on Circuits and Systems*, May 28 – 31 2000, pp. V-493 – V-496.

[28] D. Dapkus, "Class-D Audio Power Amplifiers: An Overview", *ICCE 2000, Digest of Technical Papers of International Conference on Consumer Electronics*, 13 – 15 June 2000, pp. 400 – 401.

[29] Bah-Hwee Gwee, J. S. Chang and H. Li, "A Micropower Low-Distortion Digital Pulsewidth Modulator for a Digital Class D Amplifier", *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 49, No. 4, April 2002, pp. 245 – 256.

[30] Bah-Hwee Gwee, J. S. Chang, V. Adrian and H. Amir, "A Novel Sampling Process and Pulse Generator for a Low Distortion Digital Pulse-Width Modulator for Digital Class D Amplifiers", *ISCAS '03, Proceedings of the International Symposium on Circuits and Systems*, vol. 4, 25 – 18 May, 2003, pp. IV-504 – IV-507.

[31] Olsson, T. and Nilsson, P., "Portable Digital Clock Generator for Digital Signal Processing Applications", *Electronics Letters*, Vol. 39, Issue 19, 18 Sept. 2003, pp. 1372 – 1374.

[32] Nilsson, P. and Torkelson, M., "A Monolithic Digital Clock-Generator for On-Chip Clocking of Custom DSP'S", *IEEE Journal of Solid-State Circuits*, vol. 31, Issue 5, May 1996, pp. 700 – 706.

[33] C. Wang, Y. Tseng and R Kao, "A 1.0 GHz Clock Generator Design with a Negative Delay using A Single-Shot Locking Method", *The 8th IEEE International Conference on Electronics, Circuits and Systems, 2001. ICECS 2001*. vol. 3, 2-5 Sept. 2001, pp. 1123 – 1126.

[34] C. Kim, I. Hwang and S. Kang, "A Low-Power Small Area ± 7.28-ps-jitter 1-GHz DLL-based Clock Generator", *IEEE Journal of Solid-Stage Circuits*, vol. 37, Issue 11, Nov. 2002, pp. 1414 – 1420.

[35] Woudsma, R. and Noteboom, J.M., "The Modular Design of Clock-Generator Circuits in a CMOS Building-Block System", *IEEE Journal of Solid-State Circuits*, vol. 20, Issue 3, Jun 1985, pp. 770 – 774.

[36] Fahim, A.M., "A Low-Power Clock Generator for System-on-a-chip (SoC) Processors", *Proceeding of the 30th European Solid-State Circuits Conference, 2004. ESSCIRC 2004*. 21 – 23 Sept. 2004, pp. 395 – 398.

[37] Hurst, P. J. and Rothenberg, B.C., "A Programmable Clock Generator that Uses Noise Shaping and its Application in Switched-Capacitor Filters", *IEEE Journal of Solid-State Circuits*, vol. 30, Issue 4, April 1995, pp. 403 – 411.

[38] Georgiou, G., Baeyens, et al., "Clock and Data Recovery IC for 40-Gb/s Fiber-Optic Receiver", *IEEE Journal of Solid-State Circuits*, vol. 37, Issue 9, Sep. 2002, pp. 1120 – 1125.

[39] W. Zhao, Z, Wang and En Zhu, "A 3.125-Gb/s CMOS Word Alignment Demultiplexer for Serial Data Communications", *Proceedings of the 29th European Solid-State Circuits Conference, 2003. ESSCIRC '03*, 16 – 18 Sept. 2003, pp. 389 – 392.

[40] Brynjolfson, I. and Zilic, Z, "Dynamic Clock Management for Low Power Applications in FPGAs", *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC*. 21 – 24 May 2000, pp. 139 – 142.

[41] N. H. E. Waste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Third Edition, Published by PEARSON – Addison Wesley, 2005. ISBN – 0 321 14901 7.

[42] K. K. Pahri, "Fast VLSI Binary Addition", *SIPS – 97 – Design and Implementation, IEEE Workshop on Signal Processing Systems*, 3 – 5 Nov. 1997, pp. 232 – 241.

[43] J. S. Chang, M. T. Tan, Z. H. Cheng and Y. C. Tong, "Analysis and Design of Power Efficient Class D Amplifier output Stages", *IEEE Transactions on Circuits and Systems – I*, vol. 47, no. 6, 2000, pp. 897 – 902.

[44] B. L. Sim, Y. C. Tong, J. S. Chang and C. T. Tan, "A Parametric Formulation of the Generalized Spectral Subtraction Method", *IEEE Transactions on Speech and Audio Processing*, vol. 6, no. 4, 1998, pp. 328 – 337.

[45] E. Foster, "Active Low-Pass Filter Design", *IEEE Transactions on Audio*, vol. 13, Issue 5, Sep. 1965, pp. 104 – 111.

[46] D. Meador, *Analog Signal Processing with Laplace Transforms and Active Filter Design*, Delmar – Thomson Learning, 2002. ISBN – 0 7668 2818 2.

[47] A. R. Oliva, S. S. Ang and T. V. Vo, "A Multi-Loop Voltage Feedback Filterless Class – D Switching Audio Amplifier using Unipolar Pulse-Width-Modulation", *IEEE Transactions on Consumer Electronics*, vol. 50, No. 1, Feb. 2004, pp. 312 – 319.

[48] V. M. Tousi, F. Sahandi, M. Atarodi and M. Shojaei, "A 3.3V/1W Class D Audio Power Amplifier with 103dB DR and 90% Efficiency", *Proceedings of 23rd International Conference on Micro-electronics (MIEL 2002)*, vol. 2, NIS, Yugoslavia, 12 – 15 May, 2002, pp. 581 – 584.

[49] http://ccrma.stanford.edu/CCRMA/Courses/150/SPL.html

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1. Jasbir N. Patel, Z. E. Abid, "Design of PC Programmable Digital Hearing-Testing Device", *Presented at 18th Annual Canadian Conference on Electrical and Computer Engineering*, May 2005.

2. Jasbir N. Patel, Z. E. Abid and W. Wang, "VLSI Implementation of a Floating-point Divider", *The 16th International Conference on Microelectronics, ICM 2004 Proceedings,* Dec. 6-8, 2004, pp. 505-508. ISBN: 0-7803-8656-6.