Manoj Bheemasandra Rajashekar

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Academics

Simon Fraser University, Burnaby, Canada 2022 - Present
MASc, Computer Engineering (Supervisor) Dr. Zhenman Fang, Assistant Professor

Ramaiah Institute of Technology, Bengaluru, India 2018 - 2022
BE, Electronics and Communication Engineering (Proctor) Dr. Suma K V, Associate Professor

Experience

Graduate Research Assistant, SFU (Supervisor: Dr. Zhenman Fang) Sept 2022 - Present

- Developed a novel **SpMV (sparse-matrix vector multiplication)** accelerator using Vitis HLS achieving **15x speedup** over SOTA designs on data center FPGAs, and **2x better performance per watt** compared to GPU.
- Conducted literature survey and analysis on prior designs to identify performance bottlenecks.
- Designed a novel hybrid row distribution network to effectively address workload imbalances in SpMV, crucial for **Machine Learning**, Graph Analytics, and Scientific Computing.
- Streamlined design scalability with a **Code Generator**[GitHub repo] for various FPGA configurations.

Texas Instruments, Analog Layout Design Intern, Bengaluru, India Feb 2022 to Aug 2022

- Designed constrained layouts for sub-blocks of a Motor Driver using **Cadence Tools**.
- Implemented layout techniques to address imperfections such as matching, electromigration, latch-up, etc.,
- Conducted **IR-drop and Parasitics** analysis along with **LVS/DRC** verification to ensure correctness.
- Automated layout steps using **SKILL** scripting to enhance productivity.

Samsung PRISM, Intern, Bengaluru, India July 2020 to March 2021

- Developed a **Neural Style Transfer** model for applying pre-trained art styles to images/videos.
- Implented a **Convolutional Neural Network (CNN)** model with **TensorFlow** framework, incorporating insights from research papers to design effective loss functions for style transfer.
- Quantized and ported the design to a **TFLite** model, ensuring efficient performance for Android devices.
- Successfully deployed the model on a **Flutter App** and received **Certificate of Excellence** for my work.

Controls Member, Team Phantom, SFU Oct 2023 - Present

- Joined the Controls team building **Formula-1 Electric Vehicle** at one of the university clubs.
- Developing custom HAL in firmware for **peripherals (UART, SPI, Interrupts...)** [Github repo]

Publications

- **Manoj B. Rajashekar**, Xingyu Tian, and Zhenman Fang. "HiSpMV: Hybrid Row Distribution and Vector Buffering for Imbalanced SpMV Acceleration on FPGAs". International Symposium on Field Programmable Gate Arrays (FPGA '24), Monterey, CA, USA, 2024. *(Highest review score among all the submissions)*
- **B. R. Manoj**, J. S. Yaji and S. Raghuram, "A New Constant Coefficient Multiplier for Deep Neural Network Accelerators" IEEE 3rd International Conference on VLSI SATA, Bengaluru, India, 2022.

Projects

Hotspot 2D Kernel Acceleration on Zynq7000 SoC [Github repo]

- Designed hardware accelerator for stencil operation in **Verilog**(PL), achieving **10x** speed-up over CPU.
- Developed firmware for the 2-core ARM CPU(PS), integrated Ethernet(PS) and VGA(PL) capabilities to provide data communication and user interface.

Other Projects: Articles of my hobby projects available here.

Relevant Skills

Software Programming and Heterogeneous Computing : C, C++, Python, Dart, CUDA, OpenMP
Hardware Description Languages : Verilog, SystemVerilog, High-Level-Synthesis (Vitis)